CHAPTER 1

GENERAL INFORMATION

1-1 Purpose of Equipment

The Model 401-2M12 Display Terminal, shown in Figure 1-1, is designed to provide quick response keyboard input and visual readout of information stored or processed by a General Purpose Terminal Interchange (GPTI). The display terminal operates in one of two modes: transmit or receive.

1-1.1 Transmit

In the transmit mode, display terminal operators initiate messages by operating keys on the keyboard assembly. As each character key is depressed, its associated character is produced on the cathode ray tube (CRT) screen. Simultaneously, a digital code, corresponding to the particular character, enters an internal memory device. When the operator has finished composing the message, the message is coupled through self contained interface circuits to the GPTI.

1-1.2 Receive

In the receive mode, digital data messages arriving from the GPTI are decoded by the display terminal and visual characters are produced on the CRT screen. Again, the data received are simultaneously stored in a memory device and if desired the message can be edited and returned to the GPTI.

1-1.3 Data Transfer

Data transfer between the GPTI and the display terminal is regulated by the GPTI. At the completion of message composition, the operator depresses the ENVIA key. This applies a signal to the message available line which is sent to the GPTI and inhibits all other entries by the operator. When the message available condition is recognized, the GPTI reads the data message into its core memory.

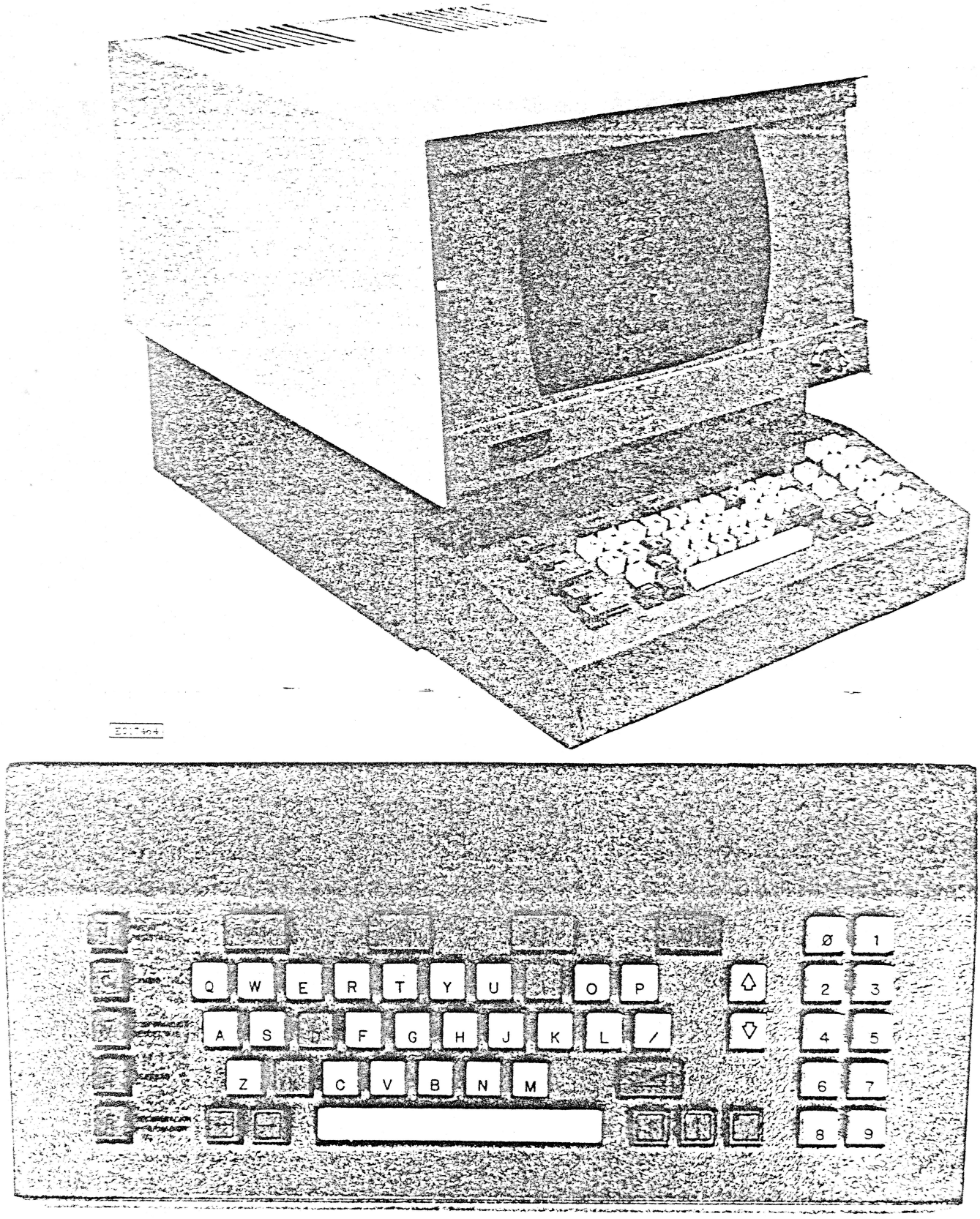

Figure 1-1. Model 401-2M12 Display Terminal

The GPTI scans the memory data for valid data lines. The valid data lines are indicated by the line tag within the horizontal retrace time of the line. Once the line tag has been found the GPTI begins accepting data from the display terminal.

After the GPTI has accepted a complete message it sends a keyboard unlock code that unlocks the keyboard and extinguishes the ENVIA light. (A list of abbreviations and symbols with their meanings appears at end of Chapter 1.) If the keyboard unlock code is not received within a predetermined time, the message is retransmitted.

1-2 Description of Unit

The Model 401-2M12 Display terminal is a compact, solid state device. The display terminal uses a monoscope as a source for character generation to produce the upper case alphabet, the numerals Ø through 9, and several special symbols. Up to 504 high-resolution characters can be displayed on the CRT screen simultaneously in a 42 character/12 line format. Editing and cursor control adds to operational flexibility by permitting operators to revise and update the information, correct errors, or arrange transmitted data messages into a particular format. All composition and editing of data messages is accomplished off-line and the display terminal is only connected to the GPTI during actual transmission.

The display terminal consists of the following major circuits and components.

a. Vertical and Horizontal Deflection Ampl. A2
b. Monoscope Deflection Amplifier A3
c. Monoscope Preamplifier A7
d. Video Amplifier A8
e. Delay Line Electronics A10

f. Keyboard Assembly A11
g. Display Logic A12
h. LVPS A4
i. HVPS A5
j. HV Network A6

1-2.1 Vertical and Horizontal Amplifier A2

The vertical and horizontal deflection amplifier assembly, shown in figure 1-2, produces sweep voltages for scanning the CRT screen. Vertical and horizontal drive signals are developed by display logic board A12. These drive signals are amplified by the deflection amplifier and two outputs are produced: vertical and horizontal sweep signals. The horizontal sweep signal causes the CRT electron beam to scan from left to right across the screen. The vertical sweep signal causes the CRT electron beam to scan from the top of the screen to the bottom. This electrostatic deflection is accomplished by the vertical and horizontal windings of a deflection coil (yoke) mounted on the CRT neck between the cathode and anode elements.

1-2.2 Monoscope Deflection Amplifier A3

The monoscope deflection amplifier, shown in figure 1-3, is used to convert digital codes to analog voltages for positioning the monoscope beam to a specific character. Six-bit digital codes are coupled from the display logic board and converted to produce two analog voltage outputs. These analog voltages are then amplified and applied to X and Y deflection plates for directing the monoscope beam to a specific character on the monoscope target.

1-2.3 Monoscope Preamplifier A7

The monoscope preamplifier circuit, shown in figure 1-4, accepts low-level video from the monoscope target and amplifies this video to a level suitable for driving the video amplifier.

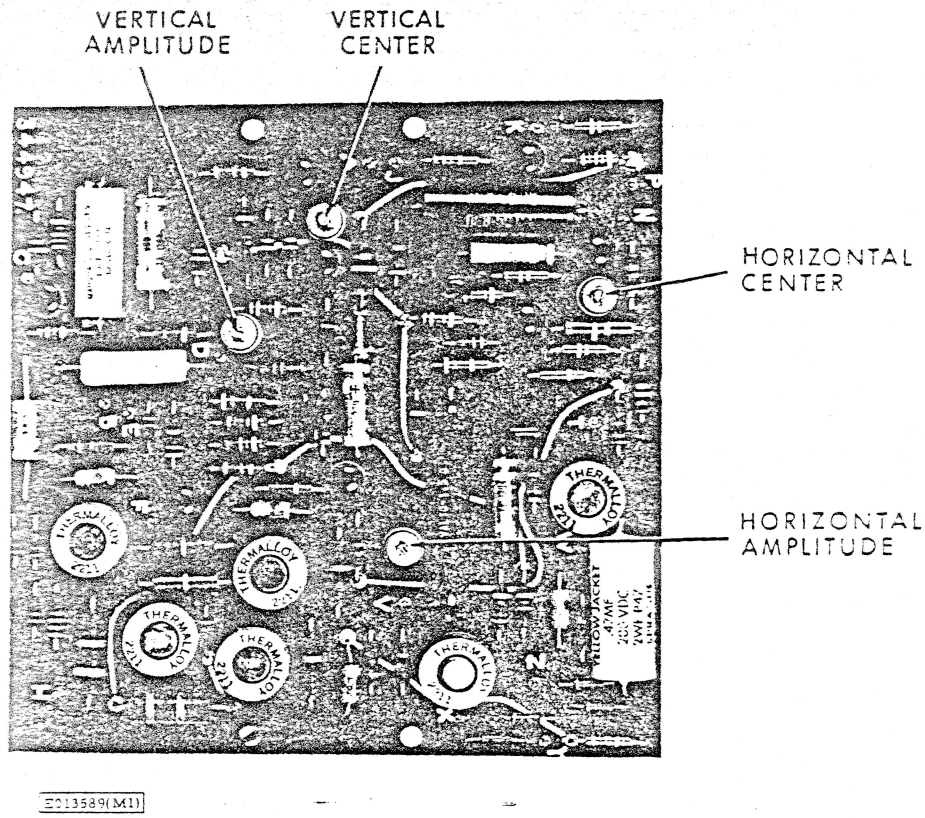

Figure 1-2. Horizontal and Vertical Deflection Amplifier A2

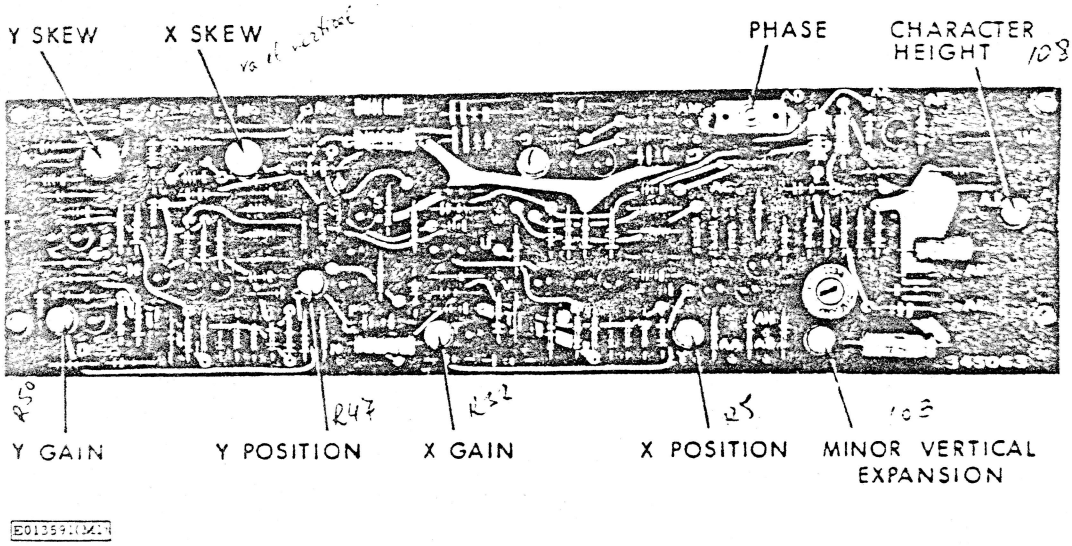

Figure 1-3. Monoscope Deflection Amplifier A3

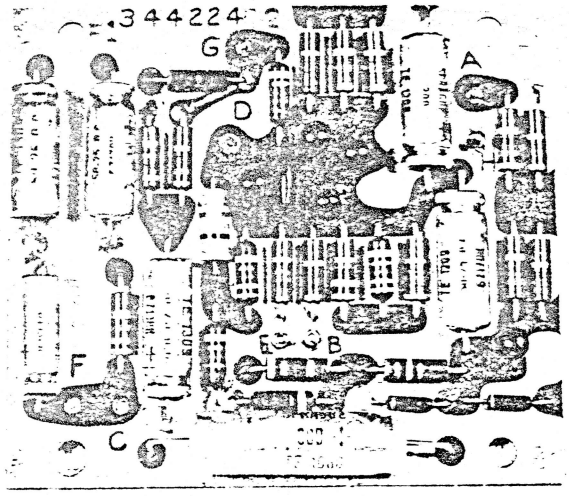

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Figure 1-4. Monoscope Preamplifier A7

1-2.4 Video Amplifier A8

The video amplifier, shown in figure 1-5, accepts the amplified video output of the preamplifier and amplifies the video signal to a level suitable for driving the CRT cathode element. In addition to amplifying video signals, the video amplifier is responsible for blanking (cutting off) the CRT screen during horizontal and vertical retrace. In this manner, the life of the CRT is prolonged and a clearer display presentation is provided.

1-2.5 Delay Line Electronics A10

The delay line electronics board, shown in figure 1-6, consists of a read-write amplifier circuit. The amplifiers in this circuit serve to amplify data coupled to and from the delay line sections to compensate for any delay line attenuation encountered by data bits.

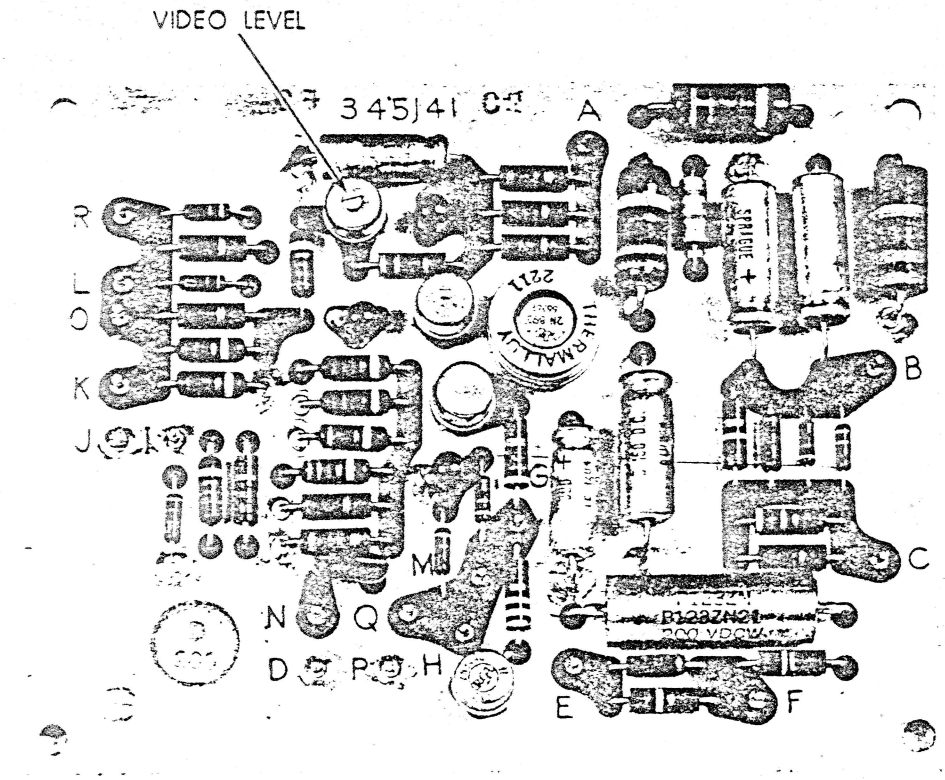


Figure 1-5. Video Amplifier A8

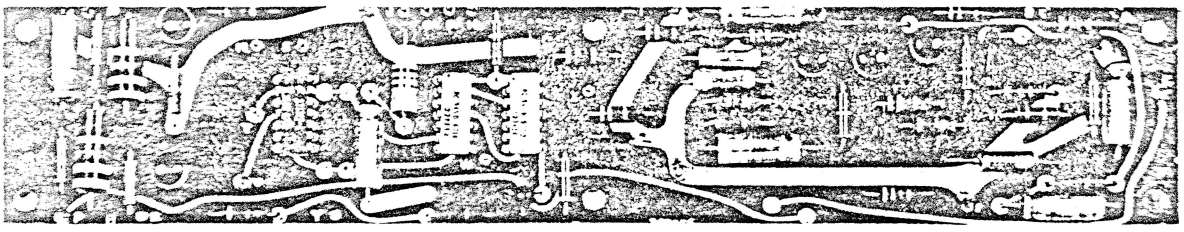


Figure 1-6. Delay Line Electronics A10

1-2.6 Keyboard Assembly A11

The keyboard assembly provides a means of initiating and editing data messages and for controlling various display terminal operations. The keyboard layout is shown in figure 1-1. The keys contained on the keyboard are:

- Upper case alphabet, plus slash symbol
- Numbers Ø through 9
- Major operation keys
- Cursor keys (keys for positioning the cursor)
- Function keys
- Transmit key

Noise free operation is provided by magnetically actuated reed switches which enable current flow through a specific branch of a self-contained diode matrix. The keys have touch characteristics similar to a high quality electric typewriter.

1-2.7 Display Logic Board A12

The display logic board, shown in figure 1-7, is a hinged printed circuit board located on the right side of the unit. Logic circuits contained on this board are formed by Diode-Transistor Logic (DTL) integrated circuits which are solder connected to etched copper printed circuits. The display logic board is composed of digital circuits responsible for the keyboard entry of data, editing and cursor control, GPTI interface and timing.

1-2.8 High Voltage Power Supply A5

High voltage power supply A5 is a compact, solid state unit which produces regulated voltages of +12 kvdc, +500 vdc, and -1.2 kvdc.

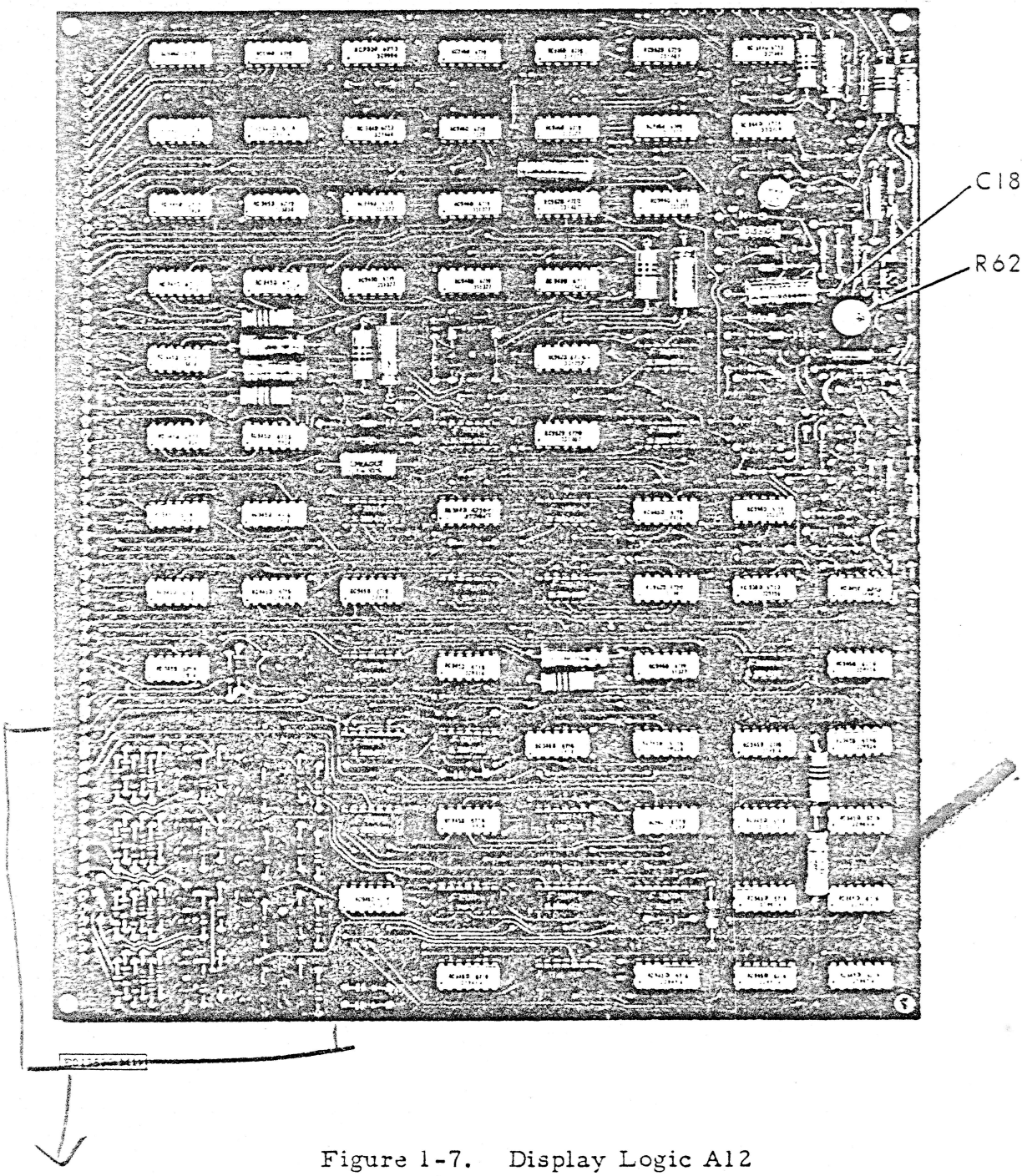


Figure 1-7. Display Logic A12

en algun modelo mas moderno k tuv
yen estos transistores por integrados
pero no alteran funcionamiento.

1-2.9 Low Voltage Power Supply A4

The low voltage power supply, A4, is similar in construction to the high voltage power supply. It furnishes regulated voltages of +22, -22, +100, and +5 vdc. It also furnishes two 6.3 vac outputs. The low voltage supply operates from a 220 vac, 50-60 Hz, single phase, 200 watt input.

1-3 Information and Reference Tables

The following pages contain tables that consolidate important reference data on the Model 401-2M12 Display Terminal. The information contained in these tables is useful for installation planning.

1-3.1 Leading Particulars

Table 1-1 lists the leading particulars of the display terminal. The information contained in this table should be used during initial planning to determine the operating requirements of the display terminal.

Table 1-1. Leading Particulars

Primary Power Requirements	220 vac +10, -5% 50-60 Hz single phase
Power Dissipation	200 w
Environmental Conditions:	
Temperature Range	50 to 100 F
Humidity Range	10% to 90% (relative)
Dimensions:	
Height	15-1/4 in. (38.73 centimeters)
Width	16-1/2 in. (41.91 centimeters)
Depth	23-1/4 in. (59.05 centimeters)
Weight	93-1/2 lb. (≈ 41 kilograms)

1-3.2 Capabilities and Limitations

Table 1-2 lists the capabilities and limitations of the Display Terminal.

Table 1-2. Capabilities and Limitations

Mode of Operation	Half Duplex
Transmission Mode	Synchronous
Character Code	Modified ASCII
Display Presentation	504 characters maximum, arranged in 12 lines of 42 characters each
Character Refresh Rate	67 refresh cycles per second
Character Format	6 data bits per character
Displayable Characters	44 including numerals, upper case alphabet, and special symbols

- Si en lugar de tener la linea de retardo mecanica que figura en esta información, tiene una Ferjeta enchufable fabricada por IBERIA. entonces es que esta modificado ola ampliado a 62 - 64 caracteres por renglon
- los microcodigos son diferentes logicamente para cada uno de los casos, permaneciendo la señal de Reloj inalterable.

ABBREVIATIONS AND SYMBOLS

ASCII	American Standard Code for Information Interch
BORRA	Erase
CFR	Cursor Frame Reset
CRT	Cathode Ray Tube
CTS	Cursor Time Slot
CTS+1	Cursor Time Slot & One Bit
D/A	Digital-to-Analog
DL	Delay Line
ENVIA	Transmit
FΔ	First Word of First Line Pulse (Frame Pulse)
FIN	End of Transaction
FWL	First Word of Line Pulse
H (Drive)	Horizontal Drive
IGNOR	Ignore Transaction
I/O	Input/Output
LSB	Least Significant Bit
LWL	Last Word of Line Pulse
MSB	Most Significant Bit
NUL	Cancel
SR	Shift Register
V (Drive)	Vertical Drive
Δ	First Word of Line Pulse
⇧	Preceding Page
⇩	Next Page
⌟	Carriage Return
⌜	Frame Reset
↓	Cursor Step Down
↑	Cursor Step Up
→	Cursor Step Right
←	Cursor Step Left
_	Cursor Symbol

CHAPTER 2

INSTALLATION AND PREOPERATION

2-1 Siting Requirements

2-1.1 Location

The Model 401-2M12 Display Terminal is designed to be installed in a location that conforms to the environmental conditions specified in table 1-1, on a sturdy desk, table, or counter capable of supporting the weight of the equipment. The display terminal requires approximately 475 square inches (3064.225 square centimeters) of surface area.

2-1.2 Primary Power Requirements

The display terminal requires a primary power input of 220 vac +10-5%.

2-2 Installation Procedure

2-2.1 Unpacking Equipment

The display terminal is shipped completely assembled and ready for operation. The display terminal interface connection is provided by an input/output (I/O) cable that must be either fabricated locally or ordered from Raytheon Company. This cable provides a means for coupling data and control signals between the display terminal and the GPTI.

Unpack the shipping crates as follows:

a. Carefully open the shipping crate(s) and check the contents of each crate against the shipping list to ensure the arrival of all ordered equipment (spare parts, cables, etc.).

b. Inspect the exterior of the display terminal for any damage that may have occurred during shipment. Any damage noted should be reported immediately.

c. Check low voltage power supply A4 to ensure that it is wired for 220 vac operation.

2-2.2 Cable Requirements

The I/O cable used for connecting the display terminal to the GPTI consists of twisted pairs of shielded number 22 AWG wire and has a maximum outside diameter of 0.35 inch (approximately 9 mm). The Raytheon part number for this I/O cable is 341449. The maximum allowable length between the display terminal and the GPTI is 300 feet (91.44 meters).

Figures 2-1 through 2-6 are provided to assist in identifying and locating the printed circuit board and chassis mounted components.

2-3 Preoperational Procedures

2-3.1 Visual Checkout

Internal mechanical and electrical connections must be checked to determine if any terminal connectors or mounting screws have loosened during shipment. To gain access to these internal connections, the cover must be removed in the following manner:

a. Locate and remove the four screws securing the cover to the main chassis. Note the brightness control knob on the right side of the display terminal. To avoid damage to this knob, lift the cover up 1/8 inch (3.17 mm) and carefully slide it back until the cover is free of the chassis. Interlock switch S1 located at the rear of the display terminal must be bypassed before power is applied to the display terminal.

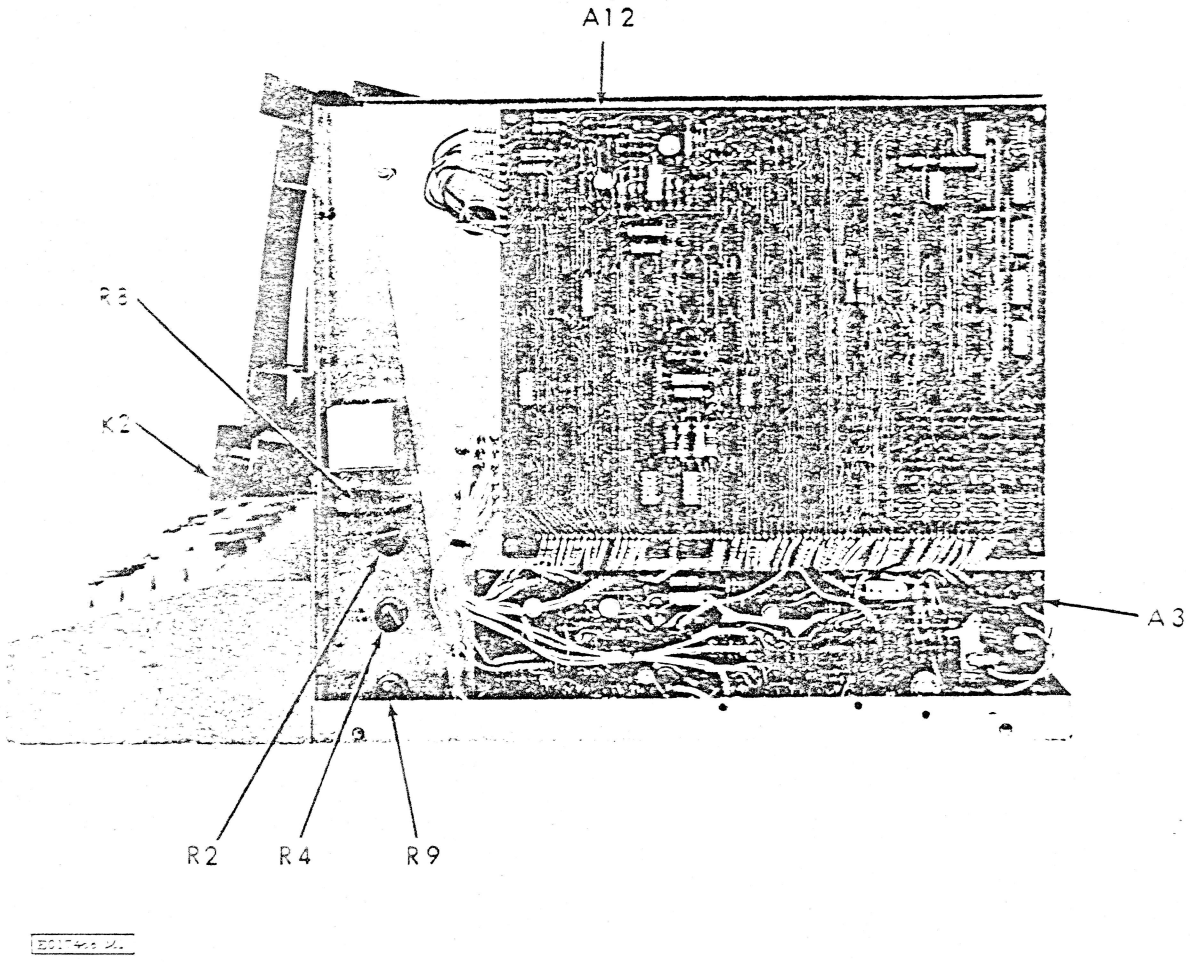
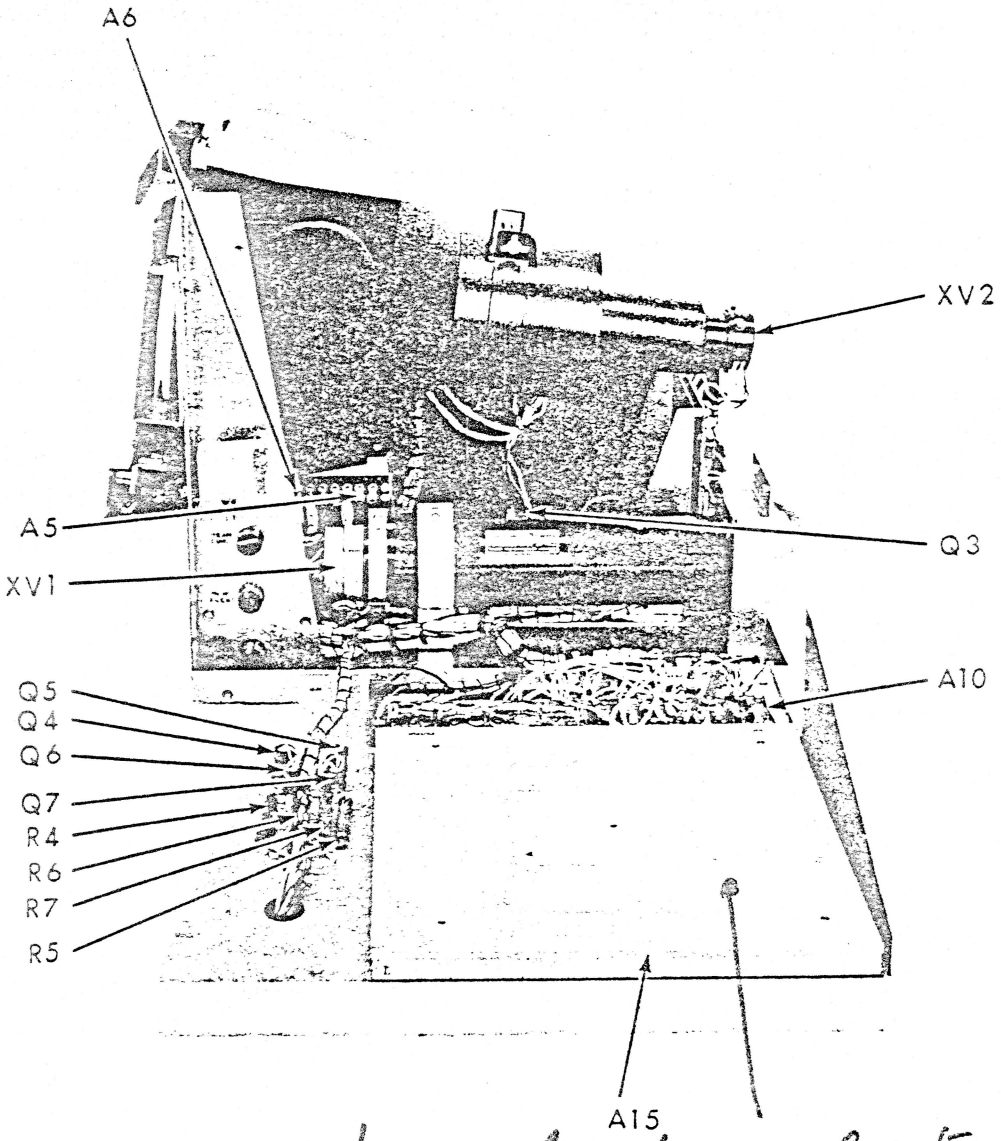


Figure 2-1. Model 401-2M12 Display Terminal, Right Side



esta es la linea de retardo
encarga a la que almacena
y que puede estar sustituida
por la tarjeta de IBERIA

Figure 2-2. Model 401-2M12 Display Terminal, Right Side Interior

lo que indica que ha sido
ampliada la memoria del
Display

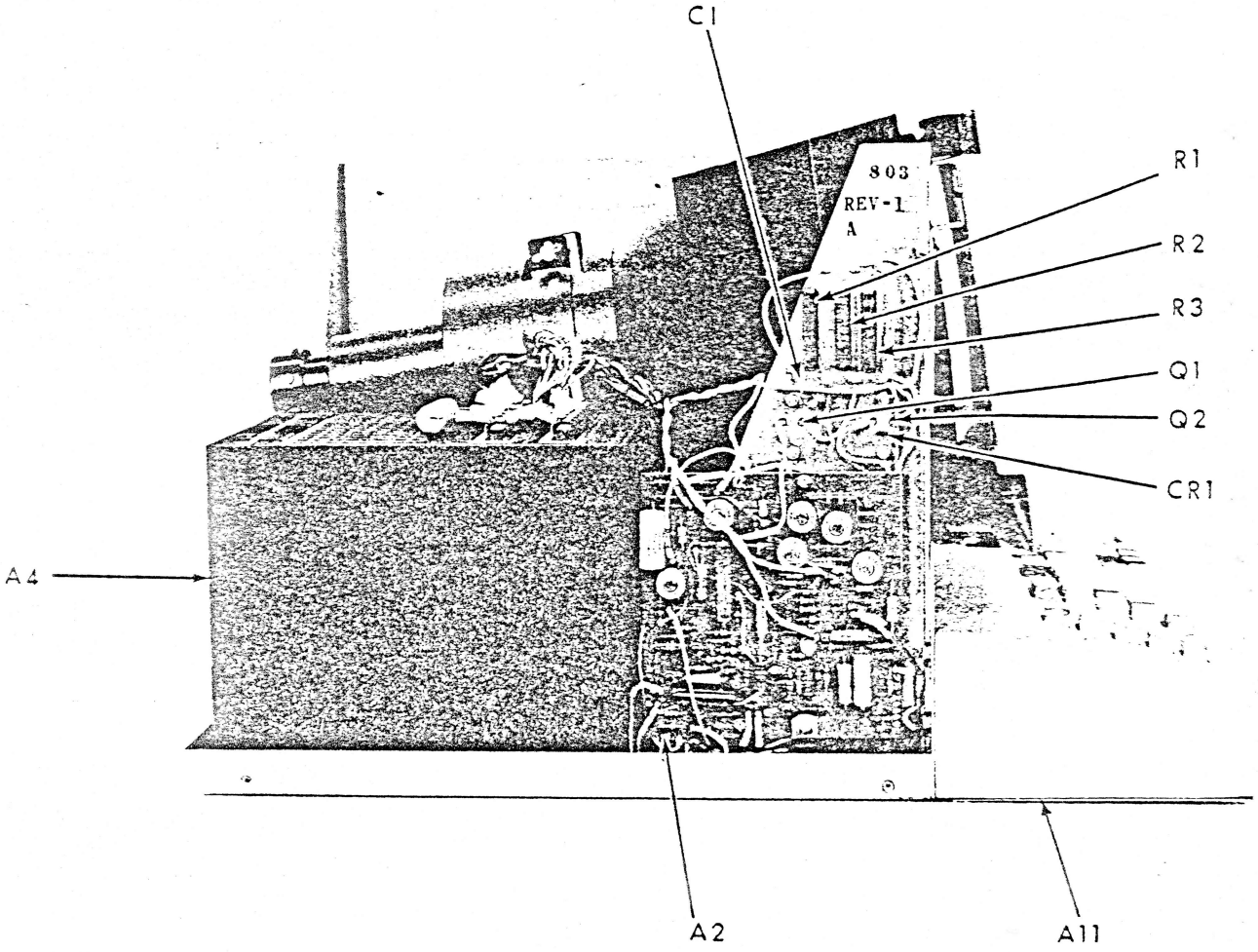


Figure 2-3. Model 401-2M12 Display Terminal, Left Side

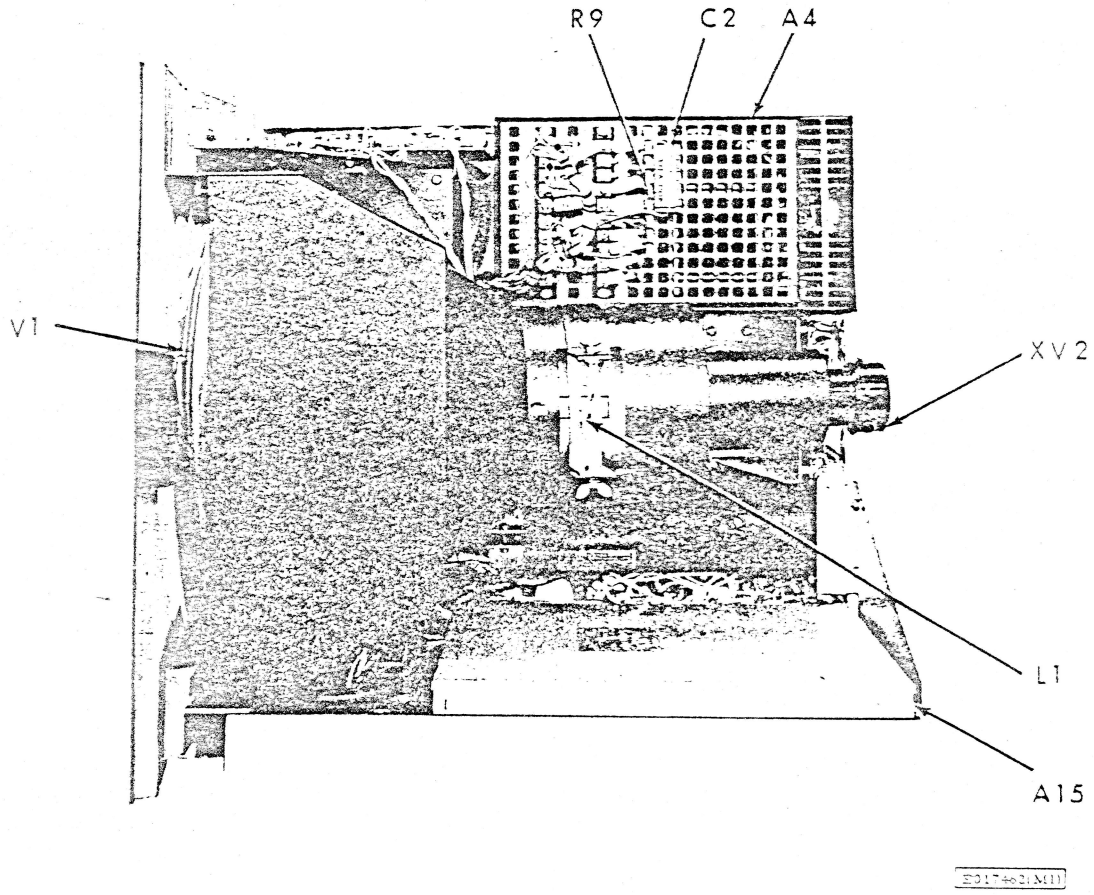


Figure 2-4. Model 401-2M12 Display Terminal, Top View

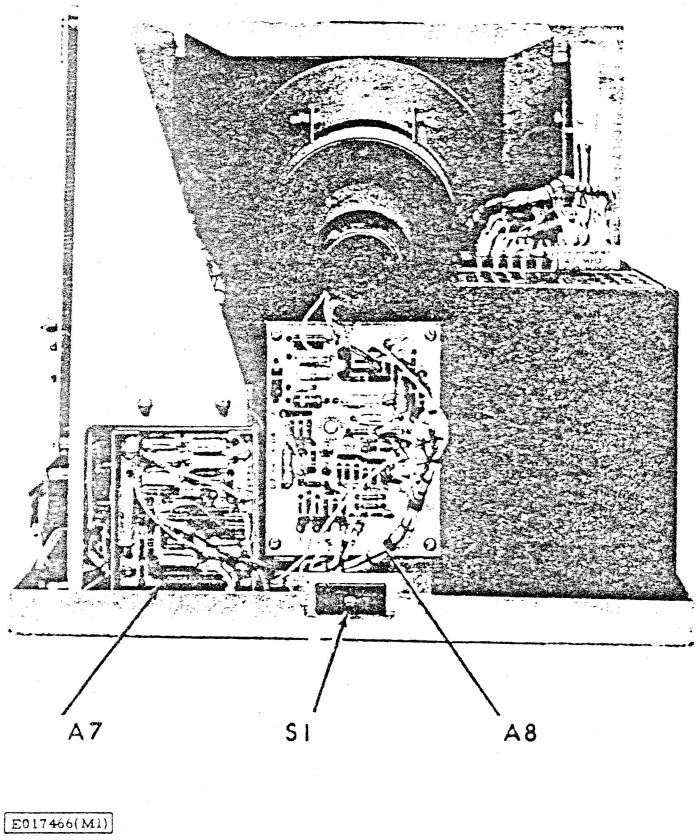


Figure 2-5. Model 401-2M12 Display Terminal, Rear View

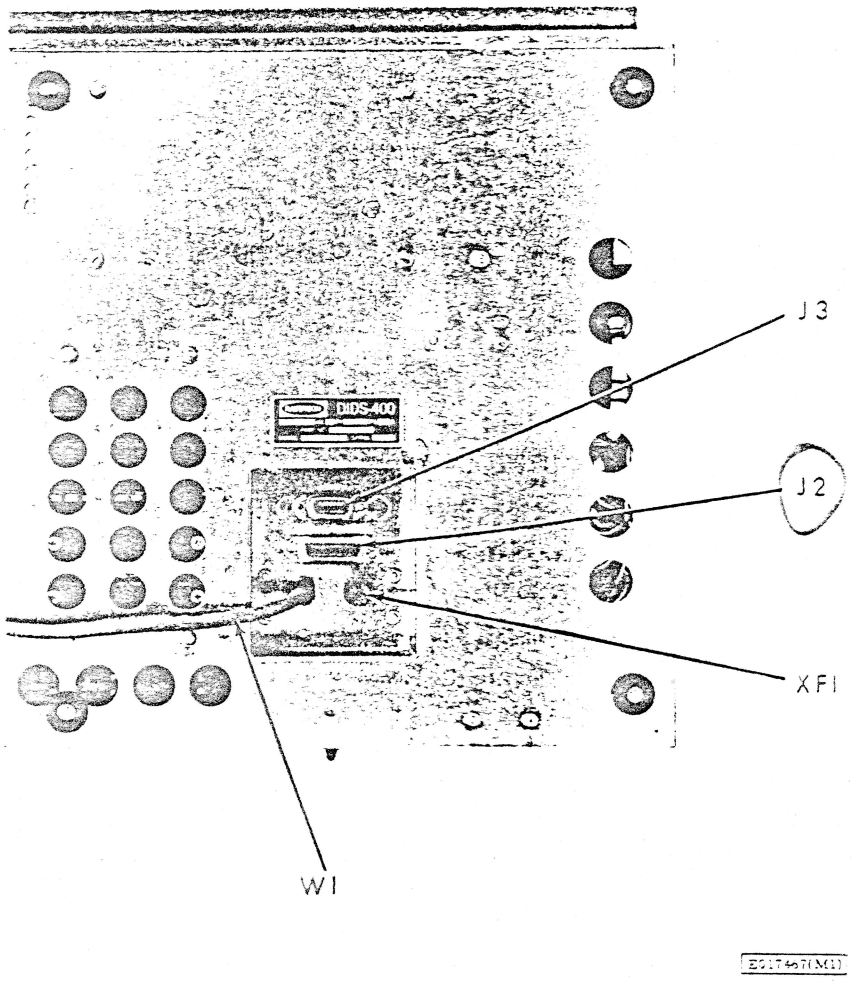


Figure 2-6. Model 401-2M12 Display Terminal, Bottom View

J2 esta conexion es la que va hacia el "modem" que envia señal de reloj y datos, si conectais algun dia este "modem" la conexion se hace el "1 con 1 el dos con dos" etc

Once the cover is removed, the internal assemblies are exposed for examination. Check the following points for good mechanical and electrical connections:

a. Check all terminal screws on both power supply assemblies.

b. Check all wiring connections to the printed circuit board assemblies.

c. Check the monoscope and CRT tube sockets to assure that they are firmly connected.

d. Check the high voltage anode lead on the CRT.

2-3.2 Resistance and Voltage Measurements

Before applying power to the display terminal, measure the electrical resistance between each power supply output line and ground. The measured resistance varies depending on equipment control settings and component tolerances. In no case, however, should the resistance to ground measure zero ohms; this would indicate a shorted condition. Careless handling during shipment could result in shorts which must be corrected before applying power to the equipment.

The dc output wiring is color coded throughout the equipment in the following manner:

+5 vdc - gray

-22 vdc - purple

+22 vdc - red

+100 vdc - orange

+540 vdc - yellow

-1.2 kvdc - red (high voltage insulation)

WARNING

Do not attempt to measure the 12 kvdc CRT anode voltage with the voltmeter. This supply produces voltages which are hazardous to human life and should only be checked with a dc voltmeter equipped with a high voltage probe.

To measure the dc voltage outputs, obtain a voltmeter (Simpson 260, or equivalent) and, after assuring that the key is turned to the off position, plug the ac power cord into a convenience receptacle. When measuring the output voltages of each supply, do not leave power applied between measurements. As soon as the measurement is recorded, remove power from the unit. This will assist in preventing equipment damage if an undetected short exists in another power supply output branch.

NOTE

The -22 vdc and +22 vdc power sources should be checked first because these voltages function as a supply for the high voltage power supply assembly (A5).

2-3.3 Alignment and Adjustment Procedures

The following alignment and adjustment procedures are provided to enable the repairman to set up the display terminal for optimum performance.

2-3.3.1 Turn-On Procedure. Power is applied to the display terminal by turning brightness control R8 and ON-OFF key K2 to the ON position. After a 3 minute warmup period, adjust brightness control R8 for proper brightness. Proper brightness is indicated when the character is clearly visible under ambient lighting conditions.

2-3.3.2 Horizontal and Vertical Deflection Amplifier A2. This adjustment should only be performed when the raster is not centered on the display terminal screen or when insufficient raster height or width is present. To position the raster, properly, perform the following adjustments:

a. Adjust vertical centering control R4 (figure 1-2) to center the raster vertically on the display tube.

b. Adjust vertical amplitude control R27 (figure 1-2) to produce the frame height.

c. Adjust horizontal centering control R35 (figure 1-2) to center the raster horizontally on the display tube.

d. Adjust horizontal amplitude control R50 (figure 1-2) to produce the frame width.

2-3.3.3 Monoscope Deflection Amplifier A3. The monoscope deflection amplifier, A3, shown in figure 1-3 should be adjusted when any one of the following conditions exists.

- Scan lines are not approximately 0.12 inch (about 3 mm) high
- Upper case alphabetical characters are not 10 percent of frame height.
- Display characters are uneven - either horizontally or vertically.
- Display characters are blurred or appear as double images.
- Display characters are not centered in their frames.

It should be noted that many of the controls interact; hence some adjustment may have to be repeated to achieve optimum alignment.

a. Adjust brightness control R8 (figure 2-1), on the side of the display terminal, until the character boxes are just visible behind the characters. Character brightness is also adjustable by means of BEAM CUR control A6-R2 on the high-voltage network. Refer to Adjustment of BEAM CUR control A6-R2 (paragraph 2-3.3.4) for proper adjustment.

b. Adjust character height control R108 (figure 1-3) until the characters are approximately 3/16 inch (4.76 mm) high.

c. Adjust minor vertical sweep expansion control R103 (figure 1-3) so that the character height is 80 percent of the visible character box height.

d. Adjust phase control C11 (figure 1-3) until single characters are produced (double characters are seen when the phase control is improperly adjusted).

e. Press the keys to display characters P W ≠ $\overline{D}$ 1 V 6 Q H 0 I N J M K L at the upper left corner of the display.

f. If the letters do not appear, adjust X and Y position controls R5 and R47 (figure 1-3) until characters ⇩ and P are visible.

g. Adjust Y position control R47 (figure 1-3) so that the character ⇩ is properly positioned within its frame.

h. Adjust Y gain control R50 (figure 1-3) until the character $\overline{D}$ is properly positioned within its frame.

i. Repeat steps g and h above until characters ⇩ and $\overline{D}$ are both properly positioned within their respective frames.

j. Adjust X position control R5 so that the character P is properly positioned within its frame.

k. Adjust X gain control R32 (figure 1-3) until the character W is properly positioned within its frame.

l. Repeat steps j and k above until characters P and W are each properly positioned within their respective frames.

m. Adjust X skew control R22 (figure 1-3) until characters Q V 1 6 are properly positioned vertically within their respective frames.

n. Adjust Y skew control R69 (figure 1-3) until characters H O I N J M K L are properly positioned horizontally within their respective frames.

o. Repeat steps i and l if necessary.

2-3.3.4 Adjustment of BEAM CUR Control A6-R2

a. Depress the keys to display a dozen or more characters.

b. Turn brightness control R8 (figure 2-1) down until the character boxes just disappear.

c. Increase BEAM CUR control R2 on circuit board A6 (figure 2-1) for the required character brightness.

2-3.3.5 Adjustment of MONO FOCUS (Monoscope Focus) Control A6-R4

a. Depress the keys to display a dozen or more characters.

b. Turn down brightness control R8 (figure 2-1).

c. Observe characters and adjust MONO FOCUS control R4 on circuit board A6 (figure 2-1) for the sharpest character presentation.

2-3.3.6 Adjustment of CRT FOCUS Control A6-R9

a. Depress the keys to display a dozen or more characters.

b. Adjust CRT FOCUS R9 on circuit board A6 (figure 2-1) for the sharpest character image.

2-3.3.7 Video Amplifier A8. Adjustment of the video level on video amplifier A8 (figure 1-5) is accomplished in the following manner:

a. Depress the BORRA key.

b. Adjust brightness control R8 and BEAM CUR control R2 for normal viewing under ambient lighting conditions.

c. Adjust video level control R7 for a 0.1 volt reading from the junction of R4 and R11 to ground.

2-3.3.8 Delay Line Adjustment. The necessity for a delay line adjustment is characterized by character shifting, flashing presentation, multiple cursors, moving characters, etc.

NOTE

Do not attempt delay line adjustments until it is absolutely established that the display terminal has had adequate time to warm up and that an adjustment is necessary. It should not be necessary to adjust the delay line more than six turns clockwise or counterclockwise from the factory adjustment.

a. Depress and release the ▭ (frame reset) key and at the same time turn the delay line adjustment screw two turns.

b. Repeat steps "a" above until the screen displays stable characters.

c. Check that the displayed characters remain stable for a minimum of three complete turns of the delay line adjustment screw.

d. Turn the adjustment screw to the center of its stable range.

2-3.3.9 Adjustment of Retransmit Control A12-R62 (figure 1-5)

a. Connect the oscilloscope probe to the + side of C18 (figure 1-7).

b. Adjust R62 (figure 1-7) for the desired length of the sawtooth. The adjustable range of the sawtooth is 4 to 35 seconds.

2-4 Initial Operation

After the display terminal is completely aligned, remove the interlock bypass and replace the display terminal cover. To determine that the equipment is operating properly, turn on the display terminal as described in paragraph 2-3.3, type in all characters, and exercise all functions. Then send a message to the GPTI which will elicit a reply that can be used to check out the receive mode of operation. If proper operation is not obtained, refer to Alignment and Adjustment Procedures (paragraph 2-3.3).

CHAPTER 3

OPERATION

This chapter is concerned with turn on, turn off, and operating procedures necessary to operate the Model 401-2M12 Display Terminal. Also included in this chapter is the name and function of all operating controls and indicators contained on the display terminal.

3-1 Identification of Operating Controls and Indicators

Table 3-1 lists the name and function of all operating controls and indicators necessary to operate the display terminal.

Table 3-1. Operating Controls and Indicators

Keyboard Notation	Name	Function
BORRA	Erase Message	Depressing the BORRA key erases all characters from the cursor to the bottom of the screen.
IGNOR	Ignore Transaction	
FIN	End of Transaction	Depressing the FIN key indicates the end of the transaction.
ENVIA	Transmit	Depressing the ENVIA key enables a message to be sent to the GPTI. Following the depression of the ENVIA key, the keyboard remains inoperable and a warning light confirms the request for transmission. When the GPTI's error free reply arrives, the keyboard becomes operable again and the warning light is extinguished.
←	Step Left	Depressing the step left key to the first detent causes the cursor to move one character position to the left. In the fully depressed

Table 3-1. Operating Controls and Indicators (cont)

Keyboard Notation	Name	Function
		second detent position, the step left function is repeated at a 6 Hz rate.
→	Step Right	Depressing the step right key to the first detent causes the cursor to move one character position to the right. In the fully depressed second detent position, the step right function is repeated at a 6 Hz rate. In either case, if the cursor is stepped to the last character of the line position, it will automatically step to the next line.
↑	Step up	Depressing the step up key moves the cursor from any character position on a line to the same character position of the line immediately above. If the cursor is in the first line when the key is depressed, the cursor will move to the last line.
↓	Step Down	Depressing the step down key moves the cursor from any character position on a line to the same character position on the next line. If the cursor is in the last line when the key is depressed the cursor will move to the first line.
⇧	Preceding Page	Depressing the ⇧ key indicates a request for the preceding page of data from the CPU.
⇩	Next Page	Depressing the ⇩ key indicates a request for the next page of data from the CPU.

Table 3-1. Operating Controls and Indicators (cont)

Keyboard Notation	Name	Function
◿	Carriage Return	Depressing the ◿ key positions the cursor to the start of the following line (all characters to the right of the carriage return symbol are erased).
▣	Frame Reset	Depressing the ▣ key positions the cursor to line 1, character 1 position.
N	Nuevo Registro	New Record
C	Cambio	Change
V	Confirmacion Derde W/L	Book from wait list
D	Separar	Divide
R	Recuperacion Informacion	Retrieve

3-2 Operating Procedures

To operate the display terminal, position the cursor to the position on the screen where the message is to begin and type in the desired text. The alphabetical and numerical characters are developed by depressing the applicable character key. A message may contain as many as 504 text characters. Each time a character key is depressed, the cursor automatically steps right.

When the message is complete, depress the ENVIA key. Depression of the ENVIA key enables the message to be sent to the GPTI. During actual transmission, the ENVIA key illuminates, indicating the keyboard is locked, and remains illuminated until the GPTI returns a parity error-free reply which unlocks the keyboard and extinguishes the light. The keyboard is again ready for further message composition as soon as it recognizes the keyboard unlock code from the GPTI.

3-3 Operating Instructions

3-3.1 Preoperational Procedures

Before initially operating the display terminal, all preoperational procedures outlined in Chapter 2 must be performed. During subsequent operation, no special preoperational procedures are necessary other than allowing a three minute warmup period before exercising any function.

3-3.2 Turn-On Procedure

To turn on the display terminal, perform the following steps:

a. Turn brightness control R8 clockwise

b. A unique key is provided to lock and unlock the power on-off switch. Turn the on-off key (K2) to the on position.

c. Allow a three minute warmup period.

d. Type in a few characters to permit a brightness adjustment. Screen brightness is increased by turning brightness control R8 clockwise until the desired eye comfort level is obtained. The CRT screen is now ready for use. It is assumed that maintenance technicians will not normally be responsible for operating the display terminal. However, after performing maintenance, especially when parts are replaced, the technician should type in the entire repertoire and exercise all functions before returning the display terminal to operation.

3-3.3 Turn Off Procedure

Turn the power on-off key to the off position.

CHAPTER 4

THEORY OF OPERATION

Section I

FUNCTIONAL DESCRIPTION

4-1 Description of Contents

This section contains information concerning the operation of the display terminal on a block diagram basis. Functionally, the display terminal can be divided into several major circuits that work in conjunction to perform specific internal functions. These circuits are grouped and described in detail with respect to purpose and functional operation.

4-2 Overall Block Diagram

The overall block diagram of the display terminal is shown in figure 4-1. The display terminal is functionally divided into the following circuits:

- Character generation and refresh
- Editing and cursor control logic
- Timing
- Raster generation
- Power supplies

4-3 Character Generation and Refresh

Perhaps the most important aspect of display terminal operation is the manner in which visual characters are developed for display on the CRT screen. While the operation of these circuits is not difficult to understand, a thorough knowledge of the principles involved is necessary to understand the various editing and cursor control functions.

The character generation circuits consist of two interrelated parts: the keyboard monoscope circuits and the refresh memory loop. The keyboard monoscope circuits convert the mechanical depression of a specific character key into a corresponding visual character on the CRT screen. The refresh memory loop periodically refreshes the display character so that a flickerfree presentation remains on the screen until the message is erased.

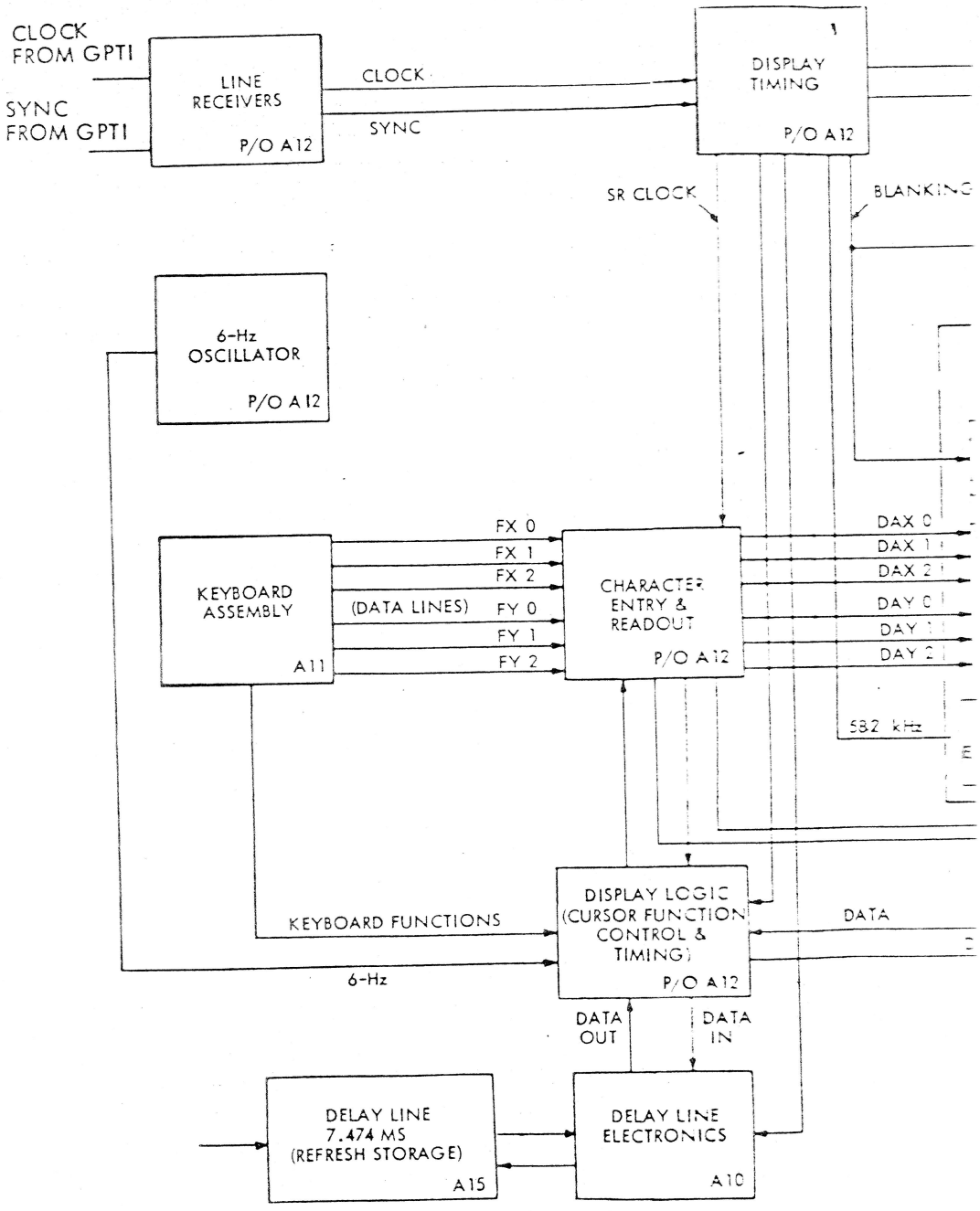
4-3.1 Keyboard Monoscope Circuits

The circuits responsible for developing visual characters for display on the CRT screen are shown in figure 4-2. The development of visual characters begins at the keyboard when the display terminal operator depresses a character key, and terminates at the CRT when a corresponding visual character is produced on the CRT screen.

4-3.1.1 Keyboard Assembly A11. The keyboard functions as a display terminal input by permitting operators to compose, format, and edit data messages for later transmission to the General Purpose Terminal Interchange (GPTI). The keyboard consists of 55 separate keys which are generally divided into two classes: character keys and function keys. The term "character keys" refers to a specific group of keys which are capable of producing visual characters on the CRT screen. The term "function keys" generally refers to those keys that do not produce visual characters on the CRT screen. Examples of function keys are keys used for editing, cursor control, and transmitting data. The function keys are listed and categorized as follows:

a. Edit key
   BORRA (Erase)

b. Cursor control keys
   - ← (cursor step left)
   - → (cursor step right)
   - ↑ (cursor step up)



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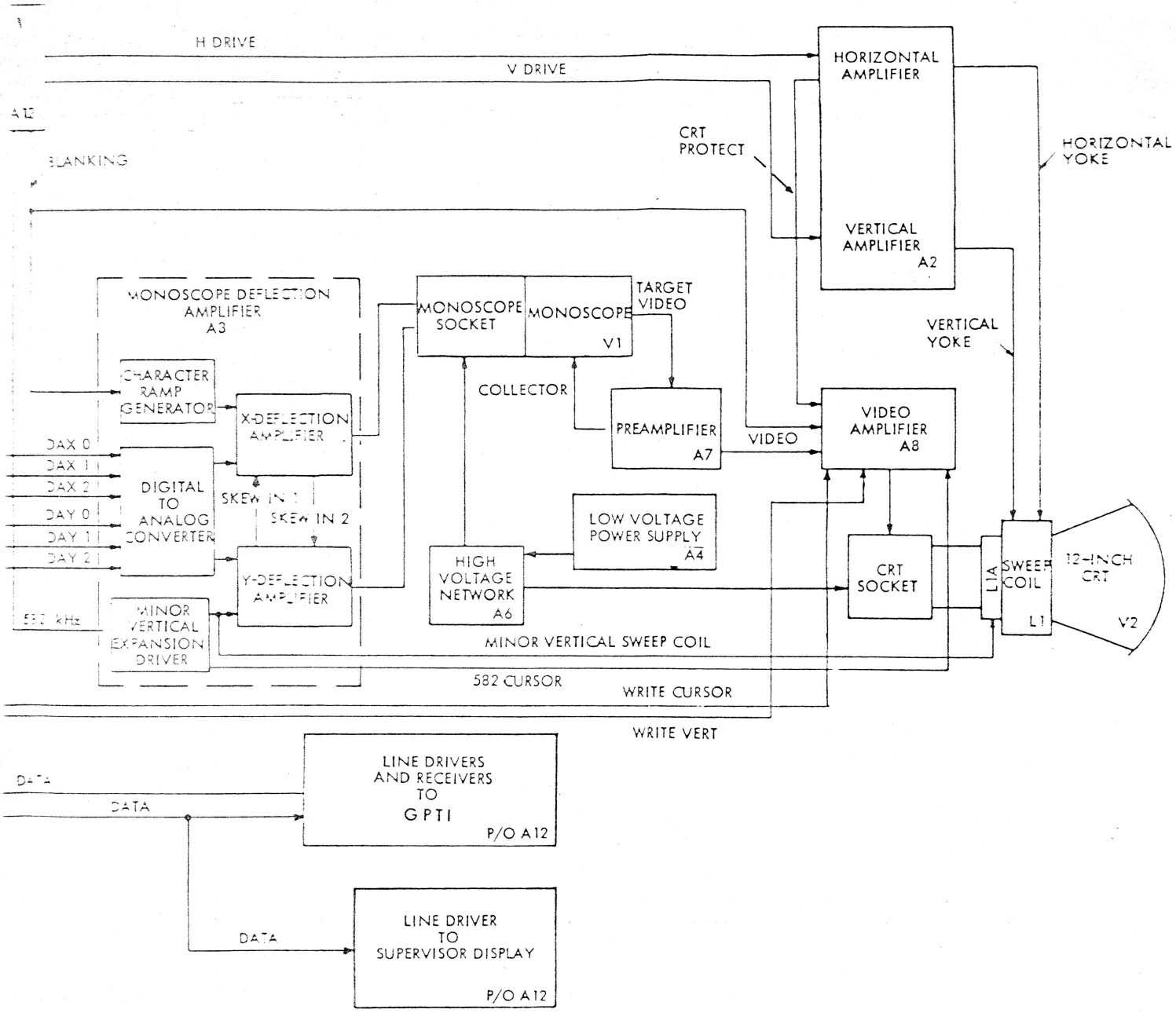
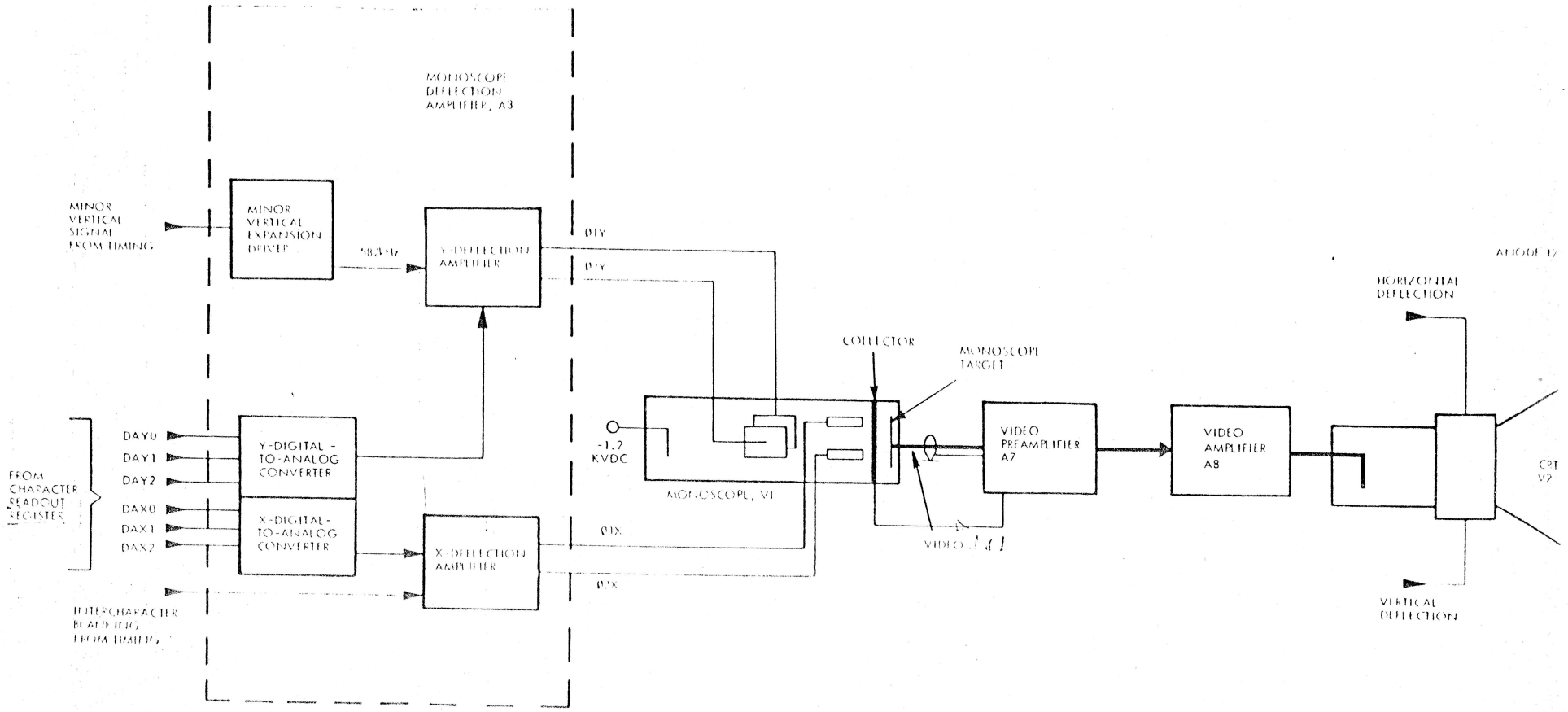


Figure 4-1. Model 401-2M12 Display Terminal Block Diagram



[DDS 68-641]

Figure 4-2. Keyboard Monos
Circuit Block Diagram

(cursor step down)
(frame reset - cursor returned to first character first line)
(carriage return)

c. Transmit keys
ENVIA (transmit)
FIN (end of transaction)
IGNOR (abort operation, ignore transaction)

d. Major operation keys

⇧	(page preceding)
⇩	(page following)
$\overline{N}$	NEUVO REGISTRO (new record)
$\overline{C}$	CAMBIO (change)
$\overline{V}$	CONFIRMACION DESDE w/l (book from wait list)
$\overline{D}$	SEPARAR (divide)
$\overline{R}$	RECUPERACION INFORMATION (retrieve)

The function of each key listed above is to perform a specific control action other than producing visual characters. With the exception of $\overline{N}$, $\overline{D}$, $\overline{R}$, $\overline{V}$, $\overline{C}$, carriage return, FIN, and IGNOR, these keys alone do not produce the digital coding necessary to develop visual characters.

When any character key is depressed, a magnetically actuated reed switch within the key allows current to flow through a branch of the keyboard matrix, figure 4-3. The matrix output, which consists of a specific 6-bit digital code, is coupled over 6 output lines designated FX0, FX1, FX2, FY0, FY1, and FY2. In addition to the digital code output a strobe pulse is produced each time a character key is depressed. This strobe pulse is used to determine that a character key has been depressed and subsequently to "strobe" the 6-bit digital code into the character entry register. The codes shown in figure 4-4 are the actual inputs to the character entry register. The character entry register is described in the following text.

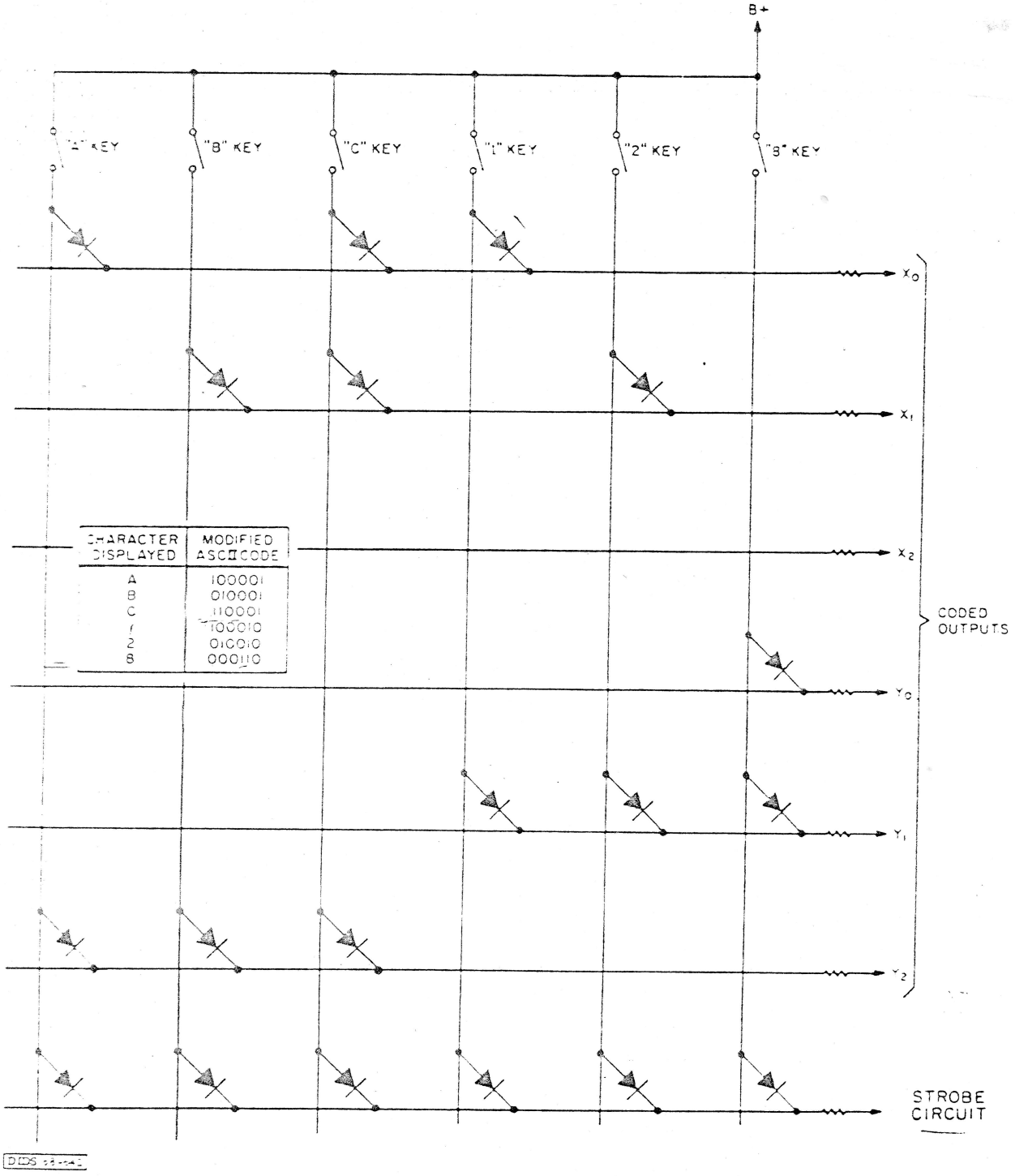


Figure 4-3. Simplified Keyboard System (Showing Part of Diode Matrix)

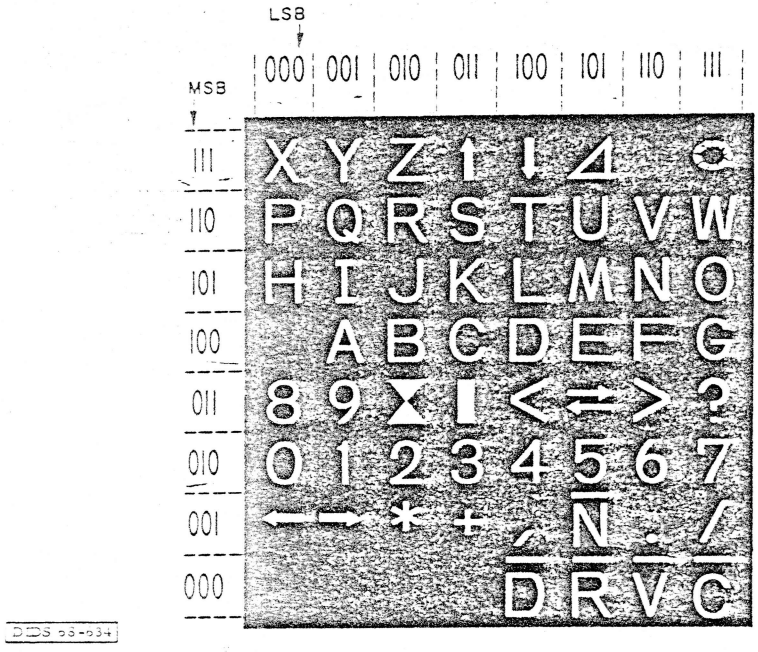


Figure 4-4. Modified ASCII Character Matrix Showing Digital Code

4-3.1.2 Character Entry Register. The character entry register, shown in figure 4-5, is a 7-bit flip-flop register contained on display logic board A12. The character entry register performs a dual function in terms of character generation: these functions are keyboard interface and refresh memory access.

When a character key is depressed, the 6-bit digital code produced by the matrix is available for character entry. However, characters can not be entered from the keyboard until a cursor and the cursor time slot (CTS) are located in the refresh memory loop. The refresh memory loop constantly circulates this bit and it only appears in the character entry register once per frame. The CTS is associated with the visible cursor on the screen and characters can only be entered at the cursor position. Thus, characters can only be strobed into the character entry register every 14.948 ms (the frame time). Since keys cannot be depressed this fast, it is practical to assume that the character code enters the register as soon as the character key is depressed. The character code is entered into the

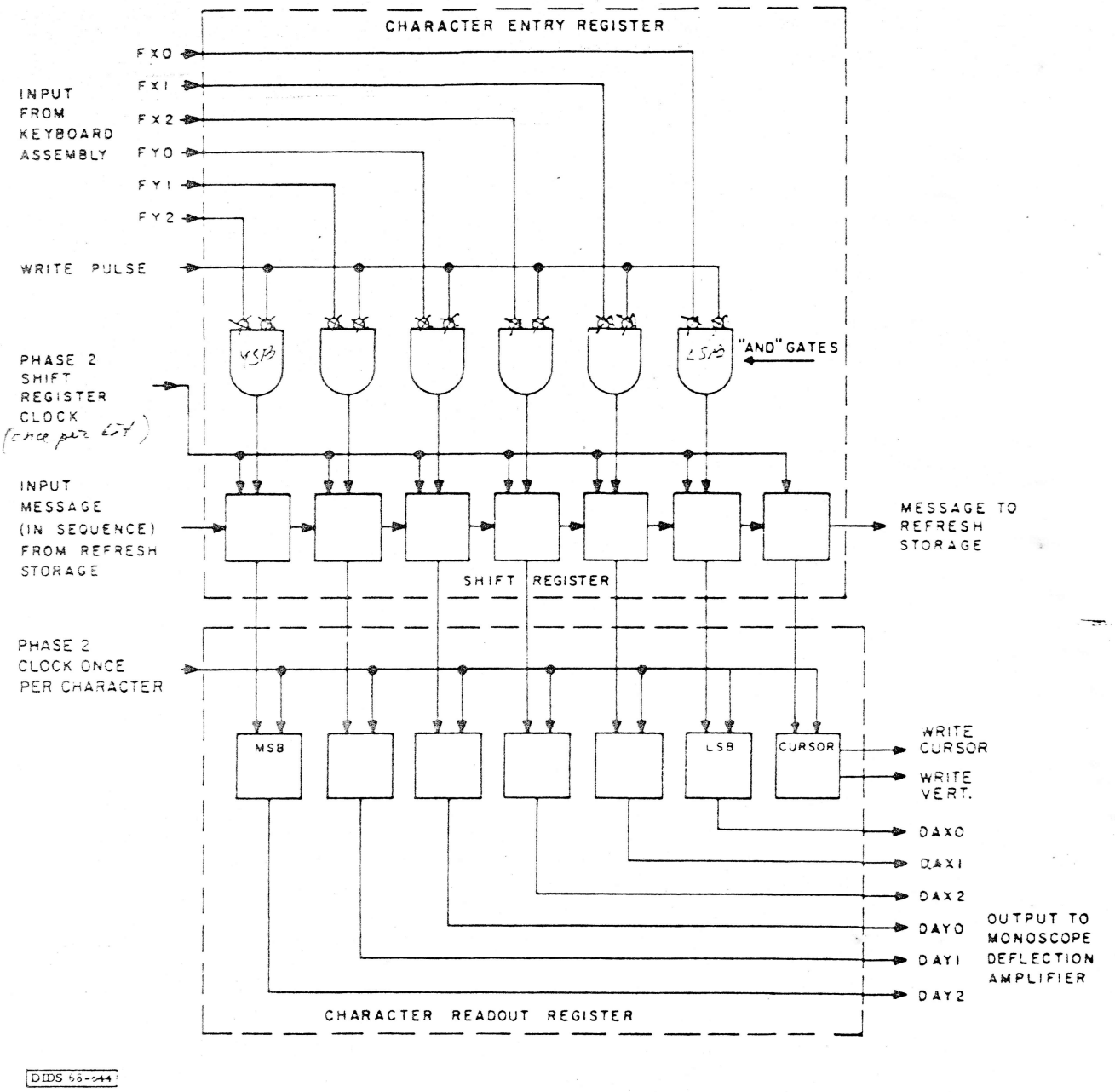


Figure 4-5. Character Entry and Readout

logic circuits by first locating the cursor and combining the presence of the cursor with the strobe pulse.

Once a character enters the character entry register, it is immediately parallel shifted into the character readout register and serially shifted, bit by bit, into the refresh memory loop.

4-3.1.3 Character Readout Register. The character readout register, also shown in figure 4-5, is a 7-bit register located on display logic board A12. The character readout register is connected in parallel with the character entry register; thus, when a character code is present in the entry register it is simultaneously present in the readout register. The character code is held in the readout register for one complete character time before being replaced with the next code entered from the keyboard (or from the refresh memory loop).

The output from the character readout register consists of the original keyboard output code divided into two segments. One segment consists of the three most significant bits (MSB's) of the character and the second segment consists of the three least significant bits (LSB's). The seventh bit of the readout register contains the cursor bit. All seven bits are coupled to the monoscope deflection amplifier and applied to X and Y digital to analog (D/A) converters.

4-3.1.4 Monoscope Deflection Amplifier A3. The purpose of the monoscope deflection amplifier is to convert digital character codes into analog voltages for electrostatically deflecting the monoscope scan. The monoscope scan, when positioned to a specific character image on the monoscope target, produces a video output by secondary emission that is peculiar to the particular character being scanned. See figure 4-6.

The three LSB's arriving from the character entry register are applied to a D/A converter to produce an X-axis deflection voltage. This voltage is amplified and applied to the monoscope X-axis deflection plates to position the scan on the appropriate column of the monoscope target front.

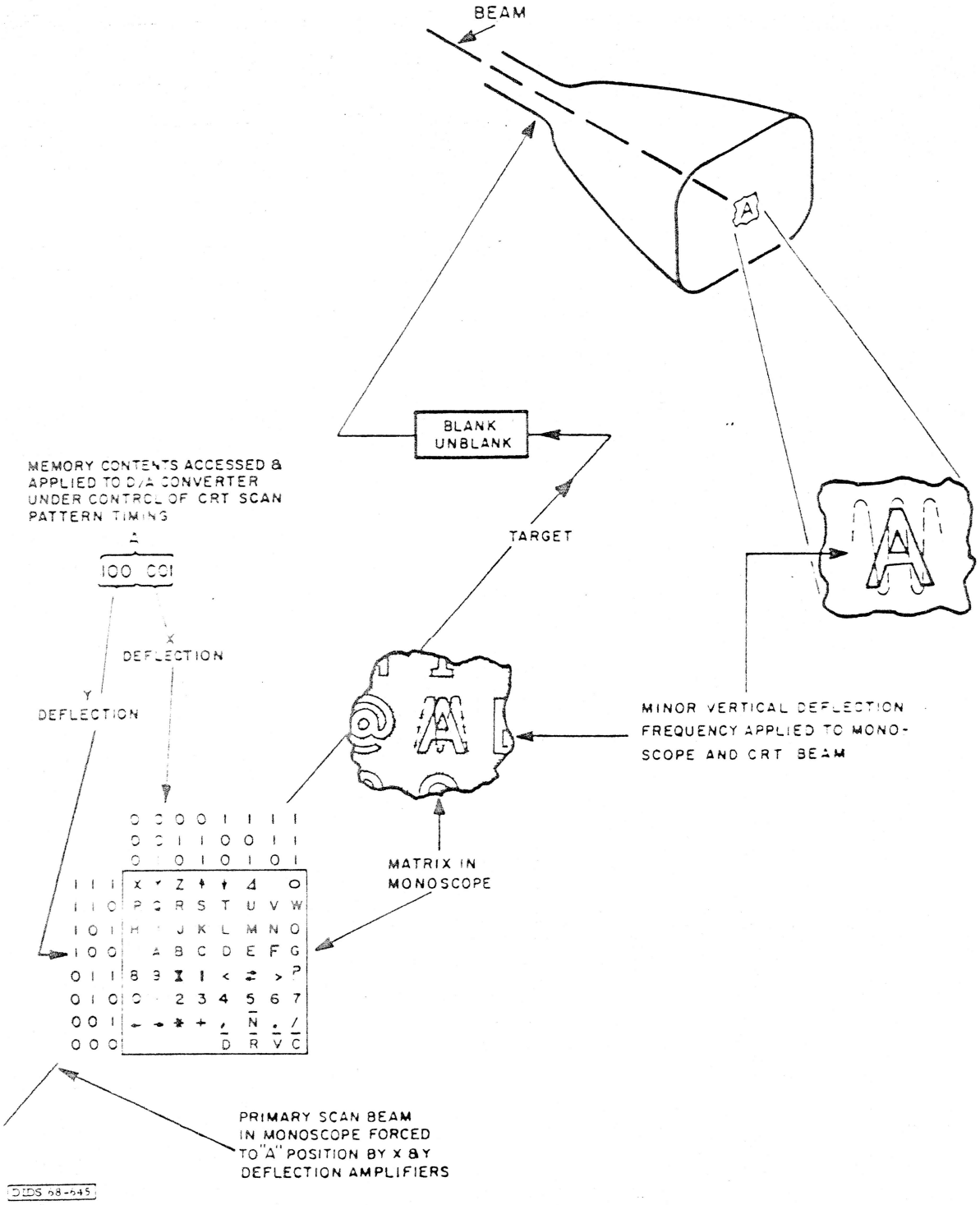


Figure 4-6. Monoscope Character Generator Technique

The three MSB's arriving from the character entry register are also converted to develop a Y-axis deflection voltage. This voltage is combined with the minor vertical expansion voltage and amplified before being applied to the Y-axis deflection plates. The purpose of the Y-deflection voltage is to position the scan to the appropriate line of the monoscope target front. Each of the 58 character images etched into the monoscope target can be accessed in this manner.

An intercharacter blanking signal is applied to the X-deflection amplifier between each character time. This signal, which is developed by the timing circuitry, cuts off the amplifier during the time elapsed when the monoscope beam is being repositioned to the next character position.

The minor vertical expansion voltage is a sine wave signal that occurs at a rate of 582 kHz. This signal amplitude modulates the Y-deflection voltage producing a composite voltage that varies at the minor vertical expansion rate. Although the monoscope scan is positioned to only one of 58 character positions, the beam itself cannot be entirely stable because of the modulating voltage. This modulating voltage causes the scan to sweep up and down alternately in a vertical direction 12 times before the scan is repositioned to another character. This "painting" motion provides a high degree of character resolution by producing a "clean" video output signal.

4-3.1.5 Monoscope Amplifiers and CRT. The monoscope amplifiers and CRT are used to develop, amplify, and display actual visual characters. The preceding text has described the method employed to position the monoscope scan to a specific position on the target while the following explanation describes what occurs when the beam is properly positioned.

The monoscope tube is a vacuum tube device designed to function similarly to a conventional electron gun. An electron beam is formed within the tube by placing a high negative potential on the cathode element and operating the collector at or near ground potential. The resulting accelerated electron beam is electrostatically deflected to bombard one

position on the target element. The target element consists of an etched aluminum disk with a character front identical to that shown in figure 4-4. As the beam is directed to a particular character of the front, secondary emission produces a weak video output peculiar to the particular character being scanned. This video signal is amplified twice by preamplifier A7 and video amplifier A8 before being applied to the CRT cathode.

The CRT is also a conventional electron gun with the anode operated at a high positive potential (with respect to the cathode element). The video level applied to the cathode alternately increases and decreases CRT conduction and the changing phosphor excitement produces a visual character on the screen. The CRT deflection voltage determines where on the screen the character will appear. Deflection voltages are developed by the display terminal timing and CRT deflection circuits.

4-3.1.6 Summary. The preceding text has briefly explained the operation of the keyboard monoscope circuits and the manner in which visual characters are developed from the depression of a character key. Once a character is displayed, however, it will begin to fade from view as soon as the monoscope scan is deflected to another character. The time required for a character to disappear is determined by the persistence of the CRT screen phosphor material which is type P31 (green) short persistence. To prevent this fading, the displayed character is refreshed by circulating the character digital code in the refresh memory loop.

4-3.2 Refresh Memory Loop

The purpose of the refresh memory loop is to provide a constant refresh of visual characters displayed on the CRT screen. The key to understanding the refresh memory loop is to remember the following two points: the character entry register is parallel connected to the character readout register; and digital character codes held in the character readout register are used to position the monoscope scan, and thus to develop a corresponding visual character on the CRT screen.

Digital character codes, whether entered from the keyboard or received from the GPTI, enter the refresh memory loop at the character entry register. If the character code is formed locally by the depression of a key on the keyboard, the code is entered by jamming it into the entry register. If the character code is received from the GPTI it is serially shifted, bit by bit, into the entry register from the data-in gating circuits. At the end of each character time, the code is serially shifted out of the entry register and into the delay line. At the same time, the character is parallel transferred into the character readout register and a corresponding character is displayed on the CRT screen. Character codes are constantly returned to the character entry register for redistribution to the monoscope deflection circuitry. This in turn maintains visual character brightness on the CRT screen.

The refresh memory loop is shown in figure 4-7 and consists of the character entry register, delay line electronics A10, and delay line A15. After a character code initially enters the refresh memory loop, the code is returned every 14.948 ms (67 times per second). This time corresponds to the time required for the CRT scan to move from a character position on the screen through a complete scan cycle and back to the original character position. For example, assume that the cursor is located at the "line one character one" position on the screen when a character key is depressed. The CTS bit associated with the cursor is constantly circulating in the loop and eventually appears in the CTS slot of the character entry register. When the cursor is located, the write pulse strobes the character code into the entry register, and a visual character is displayed on the CRT screen at the line one character one position.

The character code is then serially shifted out of the entry register until after one character time the following conditions are true: 1) the character entry register is cleared; 2) the last bit of the character code has just entered delay line electronics; and 3) the CRT scan has moved to the next character position on the screen.

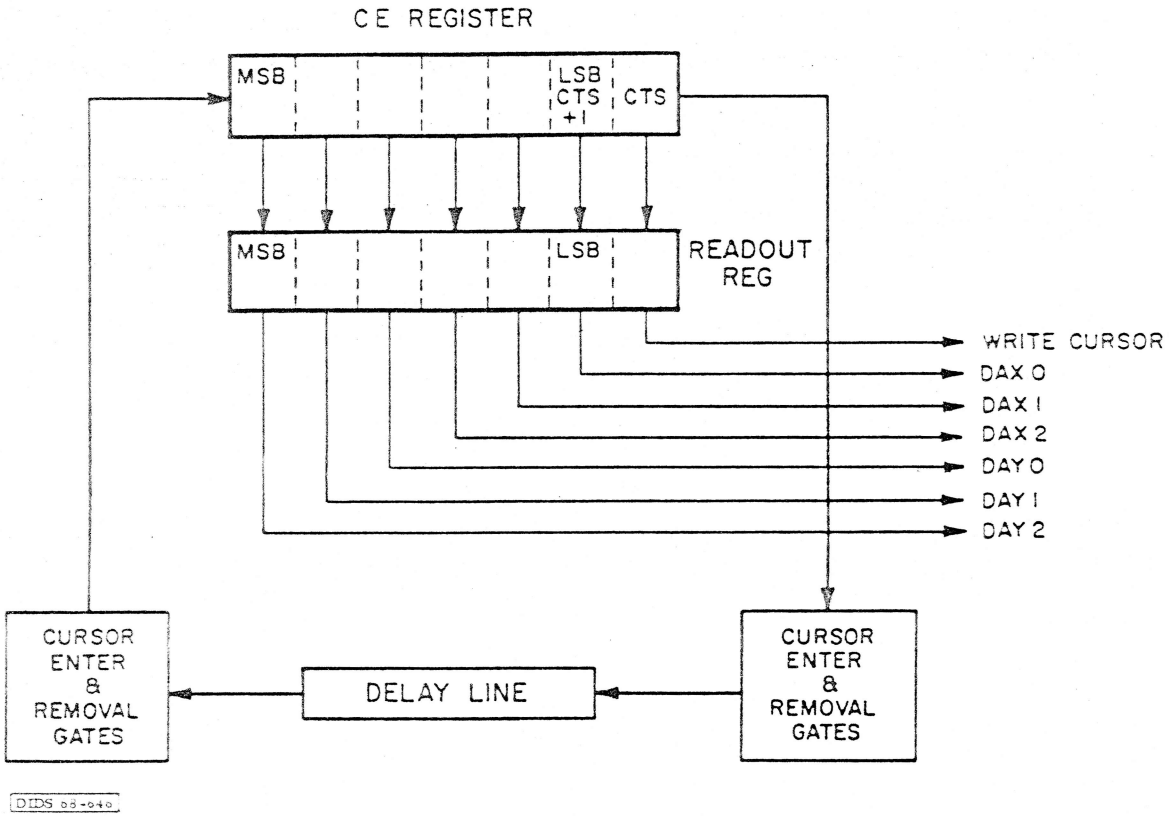


Figure 4-7. Refresh Memory Loop

In 14.948 ms, the character will be returned to the character entry register, and simultaneously the CRT scan is again at the line one character one position. Thus, the character is again visually displayed and the screen presentation is "refreshed."

4-3.2.1 Delay Line Electronics A10. The purpose of the delay line electronics is to compensate for data attenuation incurred in the delay line. The circuit consists of two amplifiers that are connected in a series configuration, one before and one after the delay line.

Serial bit data from the character entry register are applied to the write amplifier and amplified to a level sufficient to drive the input transducer of the delay line. The data passes through the delay line and appears as an

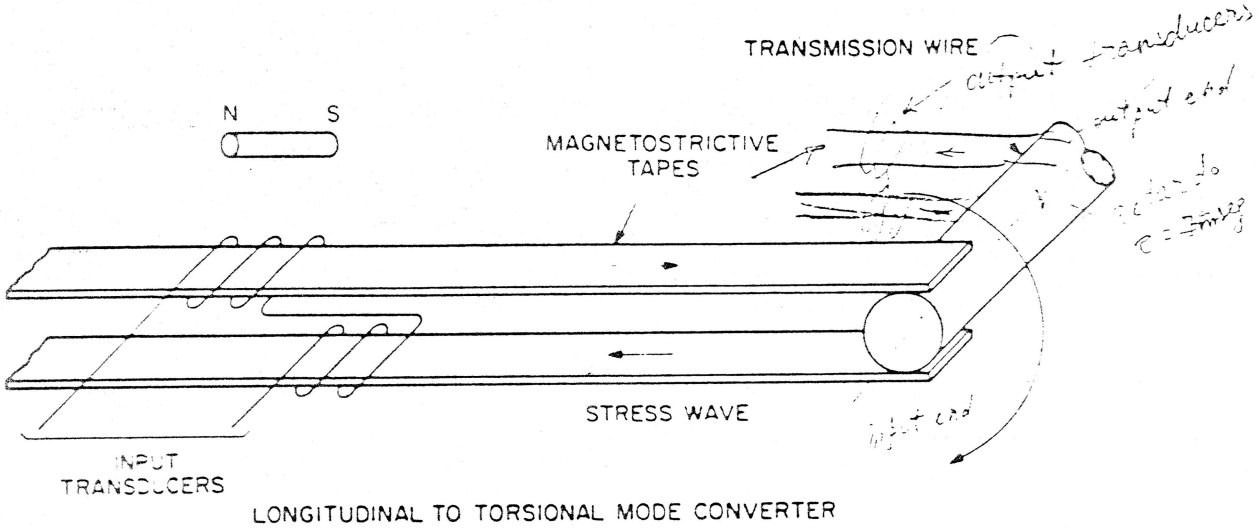
attenuated replica at the output transducer. The output of the delay line is then fed back to the input amplifier where it is amplified and recirculated through the delay line. After the data bit has circulated through the delay line twice, it is applied to the output amplifier where it is amplified and shifted into the character entry register with a delay of 14.948 ms.

4-3.2.2 Delay Line A15. The purpose of the delay line is to provide an economic means of storing up to 504 data characters and 120 retrace characters in a compact area (retrace characters are actually not characters at all but merely blank spaces in the delay line). Data characters stored in the delay line are used constantly to refresh the CRT screen presentation. In addition, during the transmit sequence, data characters are serially shifted out to the GPTI upon operator or GPTI command.

See figure 4-8. The delay line consists of the following parts: input/output transducers, magnetostrictive tapes, and transmission wire. The input and output transducers are connected to the magnetostrictive tapes which are in turn welded to each end of the transmission wire.

Data bits, in pulse form, are coupled from the write amplifier and enter the delay line at the input transducer. The transducer converts electrical energy to mechanical energy which is used to push one magnetostrictive tape while pulling on the other. The back and forth movement of the magnetostrictive tapes twists the input end of the transmission wire. This twisting motion travels down the transmission wire at a rate of 4.5 μs/inch (4.5 μs/2.54 cm) and is present at the opposite end of the wire after a certain delay in time.

At the output end of the transmission wire, the twisting movement moves a second pair of magnetostrictive tapes which couple mechanical movement to the output transducer. The output transducer converts this mechanical energy to electrical energy and the original data bit is reproduced. The total delay encountered by the pulse while traveling from the input to the output is approximately equal to 7.474 ms.



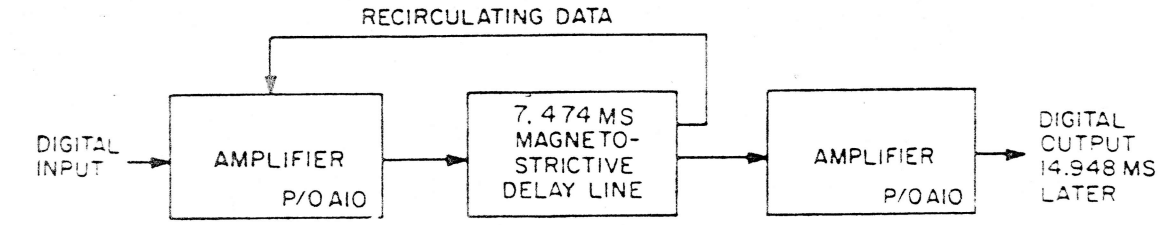


Figure 4-8. Delay Line Memory

From the output transducer data bits are fed back to the input amplifier and circulated through the delay line again in the same manner as previously described. Therefore, a total of 14.948 ms delay is encountered in the delay line portion of the refresh memory. This delay corresponds to the CRT frame time.

4-4 Editing and Cursor Control Logic

The purpose of the editing and cursor control logic is to permit operators to edit and format messages displayed on the CRT screen. These circuits are contained on Display Logic Board A12 and consist of the following principal parts:

a. Individual function flip-flops
b. Sample strobe flip-flops
c. Function complete flip-flops
d. Input and output display logic
e. Line counter
f. Character counter

In any cursor control operation, data circulating in the refresh memory loop are unaltered by the initiation of the operation. The cursor, which is a movable bit circulating in the refresh memory loop, is always attached to one character of the message. The purpose of the various cursor control operations is to locate and move this cursor from one character position to another. This repositioning may appear on the CRT screen as a cursor movement to one of the following positions:

a. Cursor stepped left or right one character position
b. Cursor stepped up or down to an adjacent line
c. Cursor moved to the frame reset position (line one, character one)
d. Advance line carriage return.

Contrary to cursor control operations, the editing operation is designed to alter in some manner the data circulating in the refresh memory loop. This alteration can appear on the CRT screen as message erase.

As shown in figure 4-9 the editing and cursor control logic can gain access to refresh memory data both before and after such data enter the delay line or character entry register. Since the character entry register is series connected in the refresh memory loop, it should be obvious that one of the 504 characters or 120 retrace characters circulating in the loop will always be present in the register. For any of the edit or cursor control operations to be initiated, the character in the register, or the character preparing to enter the register, must have the cursor bit attached to it. Previous explanations established that only one of the characters in memory has the cursor bit attached. The remaining characters, however, can

accept the cursor and this is the main purpose of the cursor control operations; to remove the cursor from one character and attach it to another.

The following text briefly describes the function of each portion of the editing and cursor control logic. See figure 4-9.

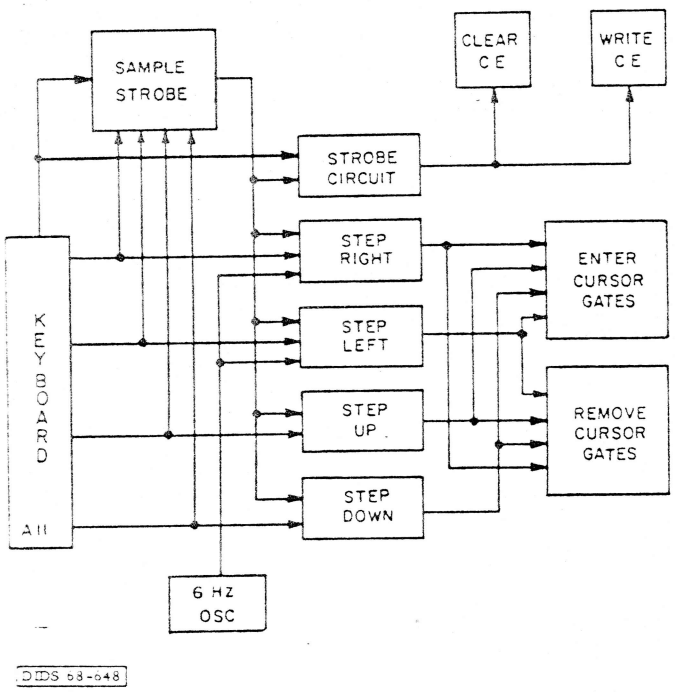


Figure 4-9. Edit and Cursor Control Block Diagram

4-4.1 Individual Function Flip-Flops

The individual flip-flops used to accomplish the various operations are normally operated independently, but in some cases are connected to other function flip-flops. An example of this is the relationship between the step right and the advance line flip-flops where the step right operation will cause an advance line if it occurs at the end of a line.

To initiate an operation, signals are coupled from the keyboard assembly. When any keyboard function key is depressed, a high to low level change is developed which is coupled to both the flip-flop associated

with the key and the sample strobe circuit. The sample strobe pulse developed by this circuit is used to clock the keyboard signal into the appropriate flip-flop.

4-4.2 Sample Strobe Circuit

The sample strobe circuit consists of a flip-flop which is used to prevent the repetition of an operation when the function key is held depressed. To accomplish this, only the first frame pulse after a key is depressed is permitted to clock the individual function flip-flop. This frame pulse is used to clock the appropriate flip-flop. For the function to be repeated, the key must be released and depressed again. The function of cursor step right or cursor step left can be made to repeat itself automatically by fully depressing the step right or step left key. With the key fully depressed, the cursor will cycle right or left at a 6 Hz rate and continue to do so until the key is released.

4-4.3 Function Complete Circuit

The purpose of the function complete flip-flop is to reset the individual function flip-flop at the completion of an operation.

4-4.4 Input and Output Display Logic

The input and output display logic consists of NAND and NOR gates both at the input and output of the delay line electronics.

Depending upon the operation initiated, data are inhibited, altered, or permitted to pass unchanged when leaving the character entry register and passing through the input display logic gates to the delay line electronics. Similar to the input display logic, the specific action taken on data leaving the delay line and preparing to enter the character entry register is dependent on the operation initiated.

4-4.5 Line Counter

The line counter works in conjunction with the step up function. The line counter is jammed to the clear state until the step up key is depressed. At this time the line counter begins to count. The line counter is toggled on each $\overline{HR}$ pulse and counts 12 lines including vertical retrace. When the 12 lines are counted a decode signal is developed. The decode is used in conjunction with the character counter to move the cursor up one line. Once the cursor has been moved up, the line counter is again jammed to the clear state.

4-4.6 Character Counter

The character counter is employed by the editing cursor control logic for each operation requiring a count of the number of characters per line. The functions requiring the line counter are step up and step down. Normally, the counter is held in the zero state by a jam signal which is applied to the jam reset input. Once the counter is instructed to count, it begins counting in binary until a count of 48 (the number of characters in a line) is decoded by the decode gate. In the step down cursor control, it is only necessary for the counter to count to 48 once. In the step up function, however, the counter continues in the sequence 0-48-0-48-etc. until the function is completed.

4-5 Timing

All the display terminal timing circuits are located on logic board A12. The internal timing consists of the various counters shown in figure 4-10. A master clock pulse at a rate of 1.1667 MHz is supplied by the GPTI, and is counted down by numerous dividers to arrive at the internal timing signals. In addition, a freerunning multivibrator is used to provide a cycling frequency of 6 Hz, for cycling selected display terminal functions.

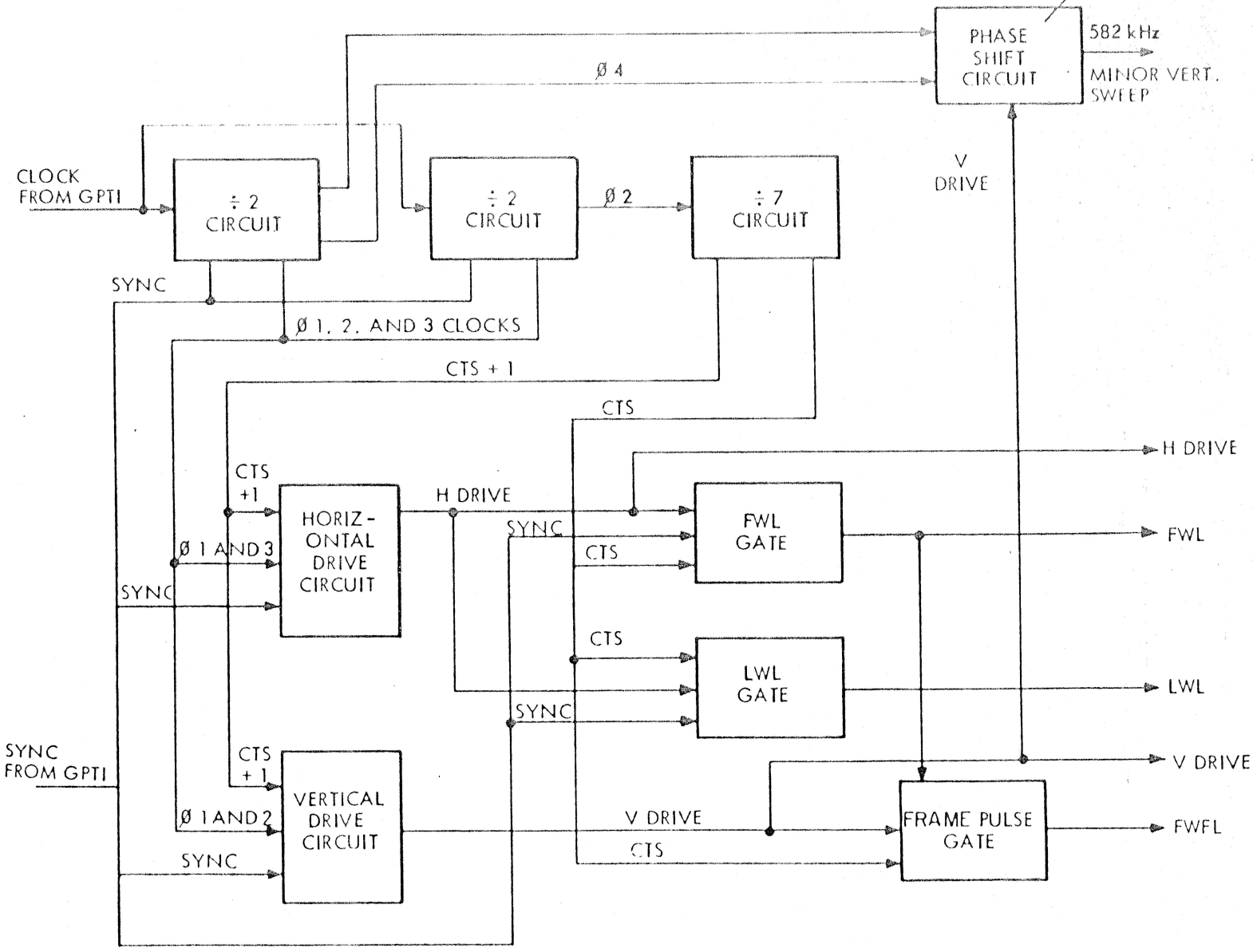


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Figure 4-10. Timing Block Diagram

4-5.1 Phase Counter

The phase counter consists of a divide-by-four counter and is formed by two flip-flops. The divide-by-four counter is toggled by the 1.1667 MHz GPTI clock. By properly combining the outputs of the two flip-flops, four phases of the master clock are developed. The phase counter produces outputs which occur in coincidence with the first, second, third, and fourth master clock inputs. These outputs are commonly known as phases 3, 4, 1, and 2, respectively. The phase counter is made synchronous with the GPTI by a sync signal which is applied by the GPTI. The sync pulses synchronize the phase counter to a count of Ø3.

Internally, the phase counter outputs are used to enable circuit operation at the beginning, middle, or end of each bit. The timing relationship is such that the time span from Ø3 to Ø2 is equal to one bit time. The Ø2 output is used within the timing circuits as a clock input to the bit counter. Thus, the bit counter is toggled at the end of each bit time.

4-5.2 Bit Counter

The bit counter consists of three flip-flops connected in a divide-by-seven count down circuit. Two outputs are decoded from the bit counter and are described as follows:

a. CTS - the cursor time slot (CTS) timing pulse is the timing equivalent to the cursor bit. From previous discussions, the cursor is a movable bit in memory which is attached to the LSB of a character. The CTS output is primarily used either to locate the cursor or to cause an operation to be performed in coincidence with the cursor.

b. CTS+1 - the "cursor time slot plus one" timing signal occurs in coincidence with the least significant data bit of a character.

4-5.3 Horizontal Retrace

The horizontal retrace pulse is used to indicate the time required for the CRT scan to retrace from the end of one line to the beginning of the next line. The horizontal retrace time is equivalent to 6 character times or 144 μs. The horizontal retrace signal may also be referred to as horizontal drive.

4-5.4 Vertical Retrace

The vertical retrace pulse is used to indicate the time required for the CRT scan to move from the last horizontal line up to the first horizontal line. This time interval is equivalent to 48 characters or 1152 μs.

4-5.5 First Word of Line (FWL) and Last Word of Line (LWL)

The first word of line and the last word of line are used to indicate the beginning and end of a line. The FWL pulse indicates when the first character of each line is to occur. The LWL pulse indicates when the last character of each line is to occur. The FΔ pulse indicates when the first character of the first line is to occur. These three pulses are generated by combinations of the horizontal drive flip-flop, vertical drive flip-flop, and sync line pulses.

4-5.6 Sync Line

Sync pulses are applied to the display terminal from the GPTI. All sync line pulses begin on a Ø3 clock and are used to force the two countdown circuits (phase counter and bit counter), to the Ø3 count, thus maintaining synchronization between the Model 401-2M12 Display Terminal and the GPTI. The sync line contains the following pulses:

- First word of line
- Horizontal retrace
- Horizontal reset
- Last word of line
- Horizontal and vertical retrace

4-6 Raster Generation

The raster is produced by exciting the CRT screen phosphor material with an electron beam. This occurs only during specific periods of time and results in the formation of 12 lines capable of containing up to 42 displayable characters each.

The electron beam used for forming the raster is developed by placing a high potential on the CRT anode element and a relatively low potential on the CRT cathode element. The high difference in potential causes electrons to leave the cathode and bombard the screen phosphor material. When the phosphor is thus excited, light is emitted to produce a visible effect. With no deflection, this light (or raster) would appear in the center of the screen as a small dot and would be useless. To produce a usable raster, the electron beam is moved about the screen by inducing deflection voltages into the yoke assembly on the CRT neck. Since the yoke is placed between the cathode and anode elements, the beam is deflected electromagnetically before it strikes the screen. By certain combinations of varying horizontal and vertical deflection voltages, the beam is swept across the screen from left to right and downwards from top to bottom. The deflection voltages applied to the deflection yoke are developed by circuits on the horizontal and vertical deflection amplifier assembly, A2, and monoscope deflection amplifier assembly, A3. The operation of these circuits is described in the following text.

4-6.1 Vertical and Horizontal Amplifier Assembly A2

The purpose of this assembly is to develop skew-corrected vertical and horizontal deflection voltages for displaying 12 horizontal lines on the CRT screen. The circuits are interconnected and operate in conjunction to produce the desired visible effect. For example, if the vertical deflection amplifier was inoperative, only one intense horizontal line would be displayed across the center of the CRT screen. Conversely, if the horizontal deflection voltages were absent, an intense vertical line would be displayed vertically at the center of the screen.

4-6.1.1 Horizontal Deflection Amplifier. The horizontal deflection amplifier receives a horizontal drive pulse from the timing circuitry. This pulse, which is active for 42 character times and inactive for 6 character times, is converted to a sawtooth waveform by a waveshaping network in the amplifier. During the active line time, the sawtooth is gradually increasing in value and moves the electron beam across the screen from left to right. At the end of 42 character times, the sawtooth rapidly collapses. This collapse allows the electron beam to return to the original position on the left side of the screen. However, since a vertical force was also exerted on the beam as it swept across the screen, the beam will begin its second horizontal excursion one line below the previous line. The CRT blanking circuit is enabled during retrace and effectively blocks the video. This halts CRT conduction during retrace and thus provides some measure of protection for the CRT phosphor material.

4-6.1.2 Vertical Deflection Amplifier. The vertical deflection amplifier receives a vertical drive pulse from the timing circuitry. This pulse, which is active for 12 line times and inactive for one line time (retrace), is converted to a sawtooth waveform by a wave forming network in the amplifier. During the active scan time, the vertical sawtooth gradually increases in value to move the electron beam from the top to the bottom of the screen. Simultaneously, the horizontal deflection voltage is causing the electron beam to produce 12 visible lines on the CRT screen. At the end of 12 line

times, the vertical sawtooth rapidly collapses which allows the electron beam to return to the top of the screen. Simultaneously, the 12th line horizontal retrace pulse is returning the beam to the left side of the screen. Thus, at the end of the 13 line times, the beam is again positioned to the top left corner of the screen (line one, character one) and a second 12 line scan is initiated.

In addition to the vertical drive pulse, the vertical amplifier receives a second input from the horizontal amplifier. A sampling of the horizontal deflection voltage is applied to the vertical amplifier and acts as a skew correction signal. As the beam scans across the screen, the increasing value of skew voltage "bucks" the vertical drive sawtooth and produces a constant vertical deflection current throughout the duration of the line. In this manner the horizontal sweep remains perfectly horizontal and no "sagging" is experienced as the horizontal scan approaches the end of the screen. The effect of this vertical compensation is illustrated in figure 4-11.

Similar to the horizontal circuitry the CRT video is effectively blocked when the vertical sawtooth collapses. This provides CRT protection during vertical retrace by cutting off the CRT for 48 character times.

4-6.1.3 Minor Vertical Expansion Signal. The minor vertical amplifier contained on monoscope deflection amplifier A3 produces an amplified 582 kHz sine wave signal. This signal is applied to the diddle coil which is also located on the neck of the CRT. The purpose of the minor vertical expansion signal is to "expand" the apparent height of the horizontal scan lines. The minor vertical expansion voltage is frequency interlaced so that during alternate CRT scans the sine wave signal will be 180 degrees out of phase. This interlacing produces a sharply defined character height.

4-7 Power Supplies

The display terminal power supply circuitry is shown in figure 4-12. Both power supply assemblies employ solid-state components to produce

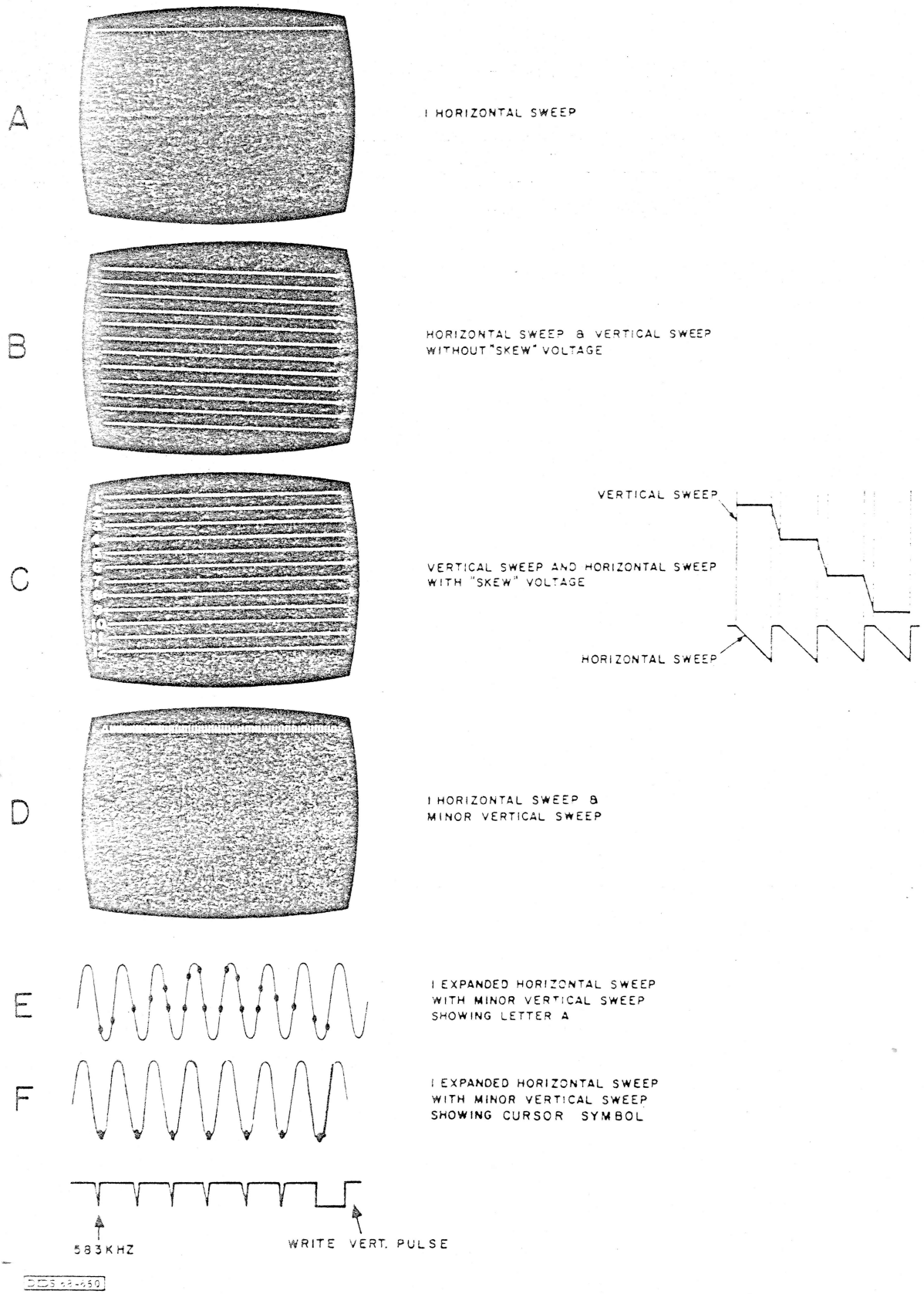


Figure 4-11. Raster Generation

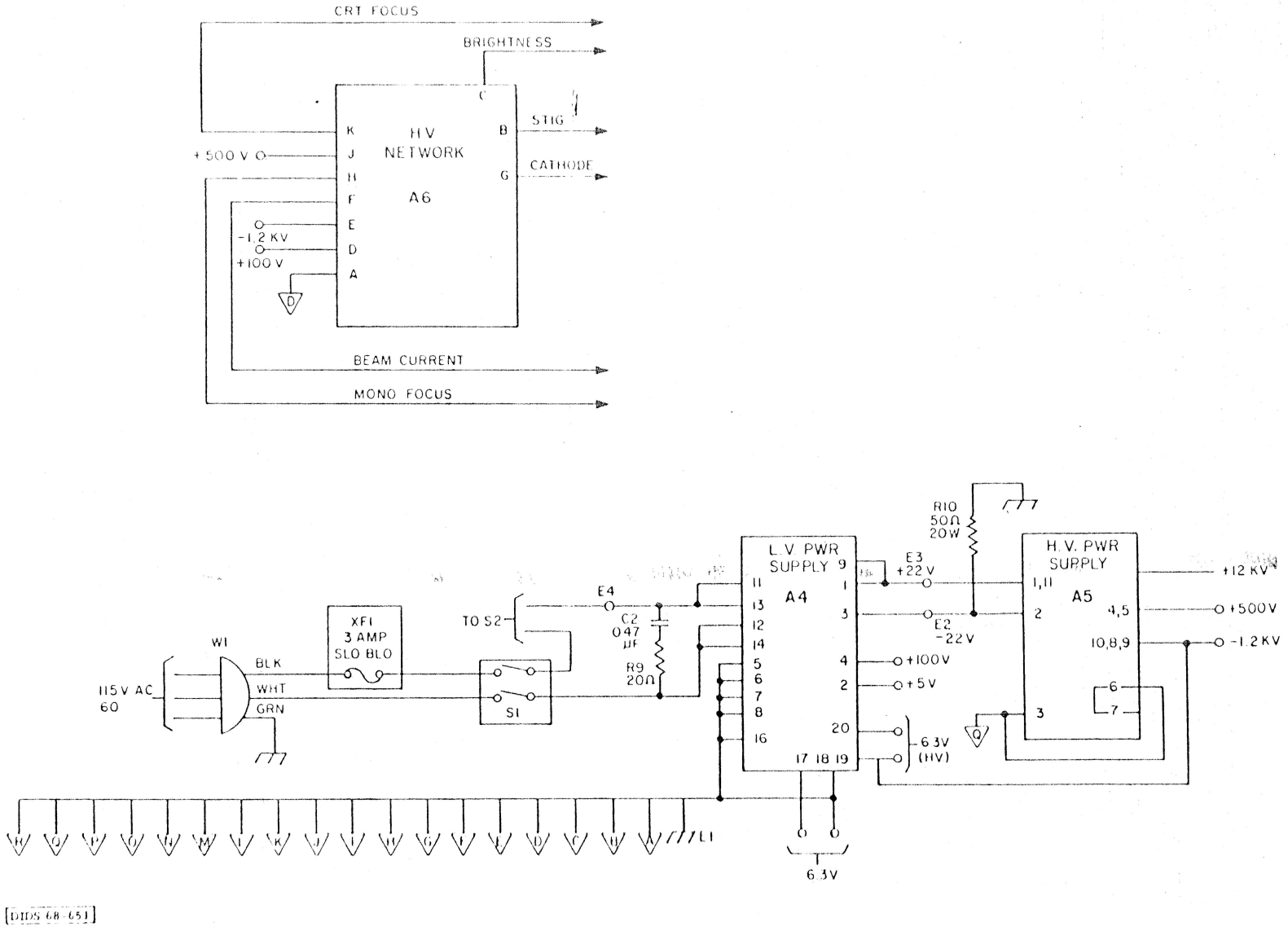


Figure 4-12. Power Supply Block Diagram

fully regulated dc output voltages. The low voltage power supply also produces two 6.3 volt ac outputs which are not regulated.

4-7.1 Low Voltage Power Supply A4

The low voltage power supply is used to develop the following output voltages:

a. +5 vdc - this voltage is used internally to operate integrated circuits located on assemblies A11, A12, A10.

b. -22 vdc and +22 vdc - these voltages are used for operating power transistors in the interface and sweep circuits. In addition, the +22 vdc and -22 vdc outputs are used as a dc source input to High Voltage Power Supply A5.

c. +100 vdc - the 100 vdc output is used for operating transistors on analog boards A2, A3, A6, and A8.

d. 6 vac (isolated) - the isolated ac output is supplied to furnish filament voltage for the monoscope.

e. 6 vac - the nonisolated ac output is supplied to furnish a filament voltage for the CRT.

4-7.2 High Voltage Power Supply

The high voltage power supply produces output voltages of +500 vdc, -1.2 kvdc, and +12 kvdc. These voltages are used for the following purposes:

a. +500 vdc - the 500 vdc output is used to furnish acceleration and focusing voltages for the CRT.

b. -1.2 kvdc - the -1.2 kvdc output voltage is applied to the monoscope cathode. This voltage enables a high difference in potential between cathode and target elements, thus producing the monoscope's electron beam.

Section II

DETAILED CIRCUIT DESCRIPTION

4-8 Timing

The timing circuits are located on the display logic board, A12, and were shown in figure 4-10 in the preceding section. The timing circuits produce timing pulses for controlling data transfer and all other internal logical operations performed by the display terminal.

All timing signals in the display terminal are originated by a master clock which is furnished by the GPTI. The master clock is at a rate of 1.1667 MHz and is applied through a line driver to the phase counter.

The timing circuits are listed and described as follows:

- Phase counter
- Minor vertical
- Bit counter
- Horizontal drive (HR)
- Vertical drive (VR)
- Last word of line (LWL)
- First word of line (FLW)
- FΔ (First character of first line)

4-8.1 Phase Counter

The phase counter shown in figure 4-13 is a divide-by-four counter which produces four phases of the master 1.1667 MHz GPTI clock. The phase counter is made synchronous with the GPTI timing by a sync pulse which is applied to the jam set input of flip-flop A16-6, and the jam clear input of flip-flop A30-6. When the sync pulse is applied, the phase counter is jammed to a Ø3 count.

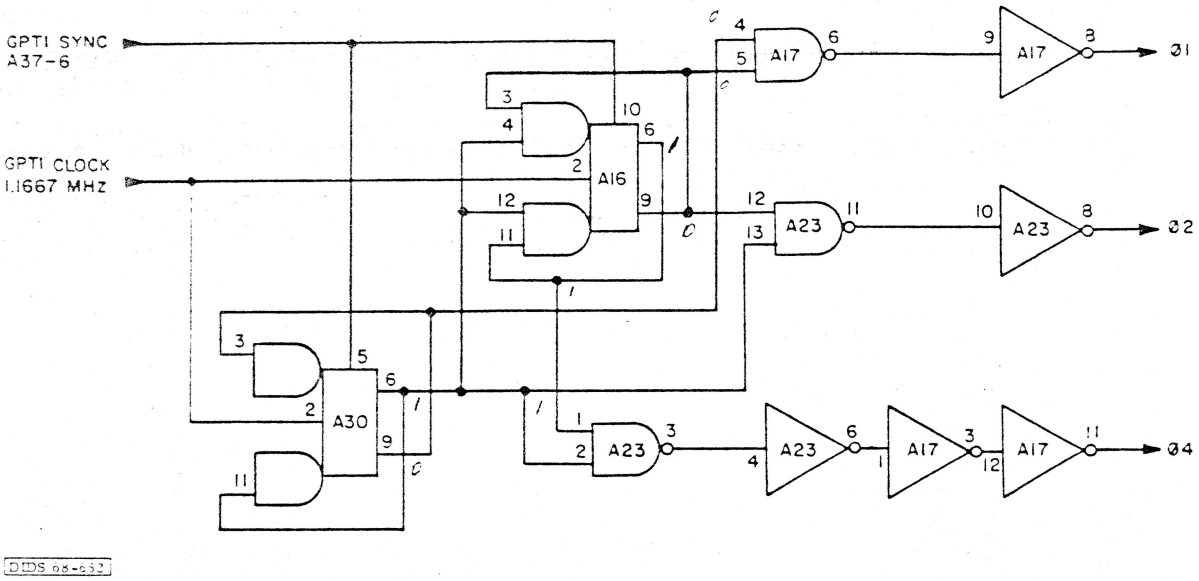


Figure 4-13. Phase Counter

The phase counter is capable of producing four different phases of the master clock: Ø1, Ø2, Ø3, and Ø4. In the Model 401-2M12 Display Terminal only three of these phases are decoded. They are Ø1, Ø2, and Ø4. Phase one is decoded in gate A17-6 and inverted by inverter A17-8. Phase two is decoded in gate A23-11 and inverted by inverter A23-8. The final decode is phase four which is decoded in gate A23-3 and then applied through three inverters. The output of the phase counter is shown in figure 4-14.

The three phases developed by the phase counter are used throughout the display terminal to perform various operations during specific periods of each bit time.

4-8.2 Minor Vertical

The minor vertical sweep circuit is illustrated in figure 4-15. The 582 kHz minor vertical sweep signal developed by a divide-by-two flip-flop A2-6, is used to produce high resolution characters of 0.17 inch (4.36 mm) in height on the CRT screen.

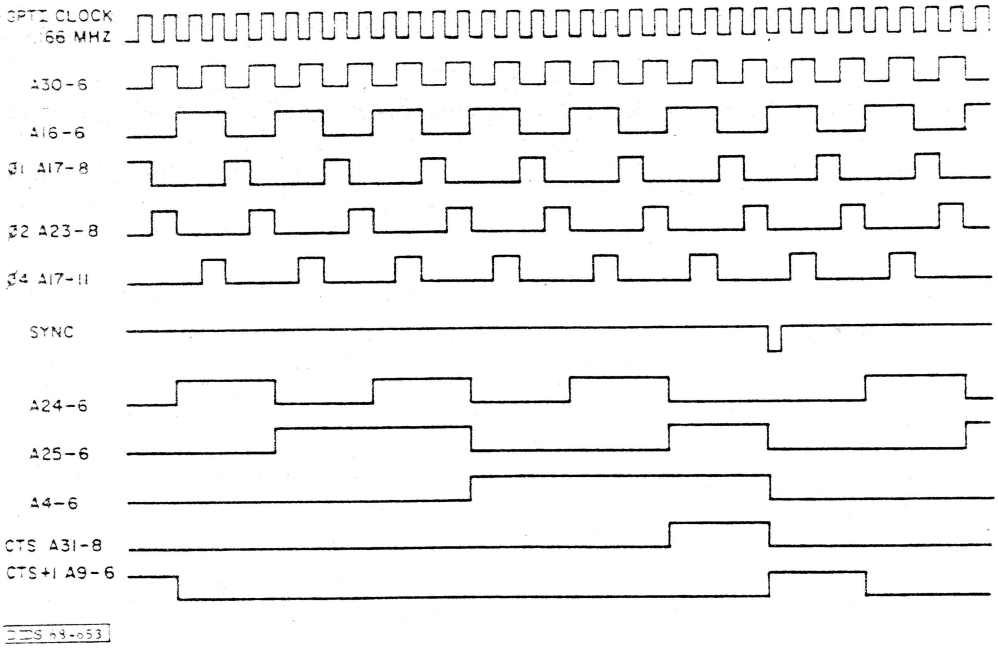


Figure 4-14. Phase and Bit Counter Timing

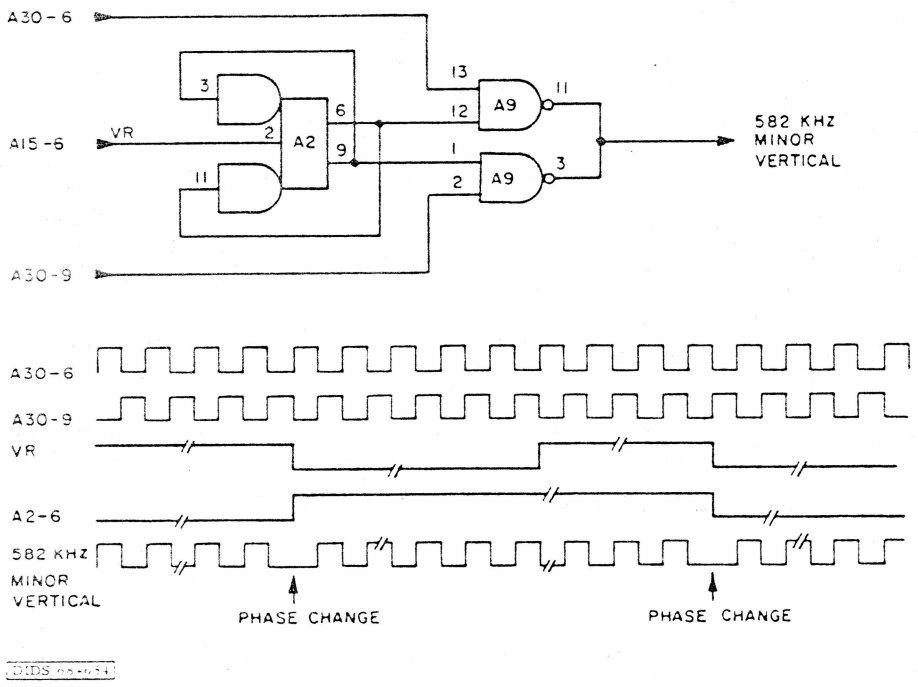


Figure 4-15. 582 kHz Minor Vertical

The minor vertical sweep circuit operates in the following manner. The divide-by-two flip-flop will change states at the end of every vertical retrace signal. The outputs of this flip-flop, A2-6 and A2-9, are applied to NAND-gates A9-11 and A9-3. Also applied to these NAND-gates is the output of the first flip-flop in the phase counter which is producing a 582 kHz signal. This 582 kHz signal is allowed to pass through one of the two NAND gates depending on what state the divide-by-two flip-flop is in. At the end of the next vertical retrace pulse the flip-flop will change states enabling the gate that was previously cut off to pass the 582 kHz signal. This 582 kHz signal is now 180 degrees out of phase with the previous minor vertical signal. This timing signal can be seen in figure 4-15.

The reason for this phase shift is illustrated by the circuits that use the minor vertical sweep signal. In the monoscope deflection amplifier, the minor vertical sweep signal is converted to a sine wave and applied simultaneously to the diddle coil and to the Y-axis deflection amplifier. At the diddle coil, the minor vertical signal "modulates" the horizontal deflection voltage and thereby creates an increased line height. By reversing the phase in alternate frames, the frequency of this modulating signal is effectively doubled and a sharper horizontal line is thereby developed. In the Y-axis amplifier, the minor vertical sweep signal causes the monoscope beam to "paint" up and down over the character being scanned. Again, a phase reversal on alternate frames essentially doubles the number of times the character symbol is "painted" and the resulting video signal more accurately defines the character being scanned.

4-8.3 Bit Counter

The bit counter shown in figure 4-16 is a divide-by-seven counter that produces two outputs: CTS, and CTS+1. The Ø2 pulses developed by the phase counter are applied to the clock inputs of A24-6 and A25-6. The third flip-flop, A4-6, is toggled each time A25-6 goes to the "clear" state.

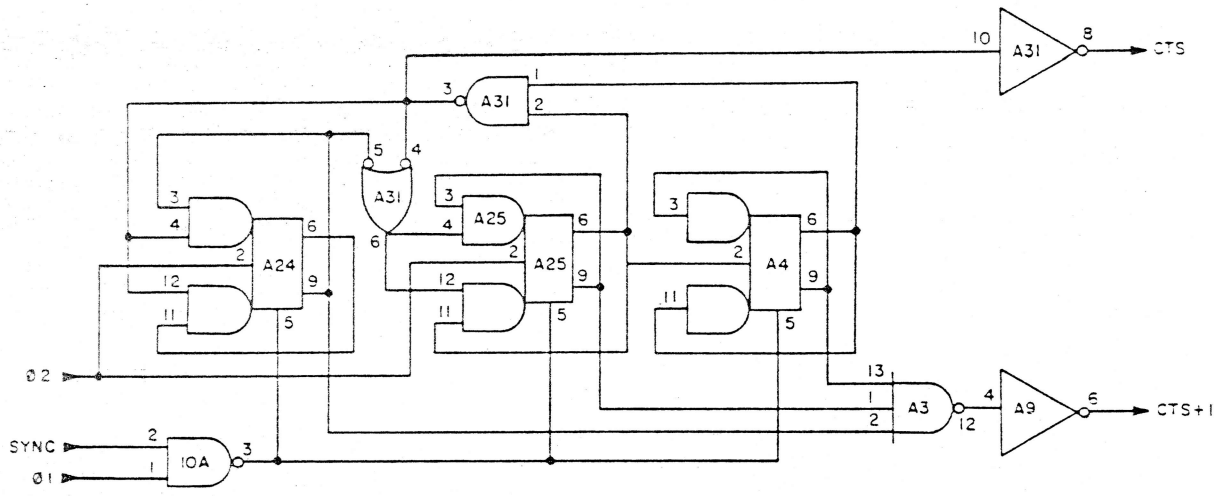


Figure 4-16. Bit Counter

The bit counter is synchronized to the GPTI timing by means of a sync pulse applied from the GPTI. The sync pulse is applied to the jam clear inputs at A24-5, A25-5, and A4-5. This jam signal will sync the bit counter to a count of CTS+1. The sync signal is developed in gate A10-3 and occurs once per line.

Once the bit counter is synchronized, the flip-flops cycle through seven repetitive counts as shown in figure 4-14. Although the counter cycles through seven distinct states, only two outputs are decoded. The CTS output is decoded in gate A31-3 and inverted in inverter A31-8. CTS+1 is decoded in gate A3-12 and applied to inverter A9-6. These outputs are used for the following purposes:

a. CTS - This output is defined as the "first" bit of a character and is in coincidence with the cursor bit in memory. The CTS decoded output is used to perform logical operations in coincidence with the cursor bit.

b. CTS+1 - This output occurs in coincidence with the LSB of the six data bits of the character. Remember, the first bit of a character, CTS, is not a data bit; therefore, CTS+1 is the LSB of the data bits.

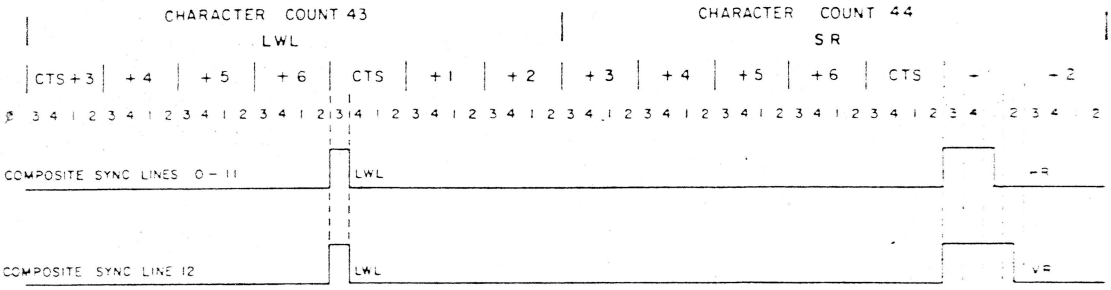
4-8.4 Horizontal Drive

The output of the horizontal drive (may also be referred to as horizontal retrace) circuit is dependent on the pulses applied from the GPTI on the sync line. Therefore an explanation of the sync line follows:

The composite sync signal (figure 4-17), is produced by the GPTI and is composed of four separate pulses:

- First Word of Line (FWL); this pulse occurs during character one at CTS, Ø3 time.
- Last Word of Line (LWL); this pulse occurs during character number 43 at CTS, Ø3 time.
- Horizontal Reset; this occurs during character number two at CTS+1, Ø3 time.
- Horizontal and Vertical Retrace (HR, VR); the horizontal retrace pulse is generated during lines 1 through 11 and occurs during character number 44 at CTS+1, Ø3, Ø4, and the first half of Ø1 time. Both the horizontal and vertical retrace pulses are combined during line 12 and occur during character 44 at CTS+1, Ø3, Ø4, Ø1 and the first half of Ø2 time.

The horizontal retrace circuit, shown in figure 4-18, is composed of one latch-type flip-flop, A10-6 and A10-8. The output from the flip-flop is a gate 144 μs wide. This gate represents the horizontal line retrace time and is equivalent to six character times. The 144 μs gates are 1152 μs apart: this represents the horizontal line time, or the time taken to enter 42 characters into memory plus horizontal retrace time.


CHARACTER COUNT 43
LWL
CHARACTER COUNT 44
SR
CTS+3
+4
+5
+6
CTS
+1
+2
+3
+4
+5
+6
CTS
-
-2
COMPOSITE SYNC LINES 0 – 11
LWL
COMPOSITE SYNC LINE 12
LWL

DDS 4A-580

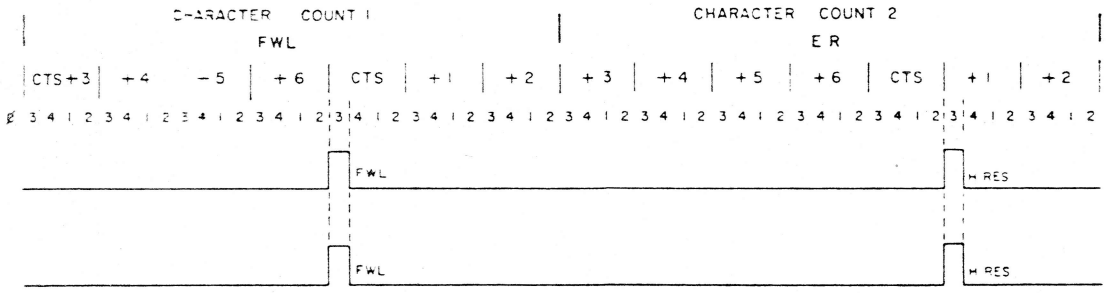


Figure 4-17. Sync Line

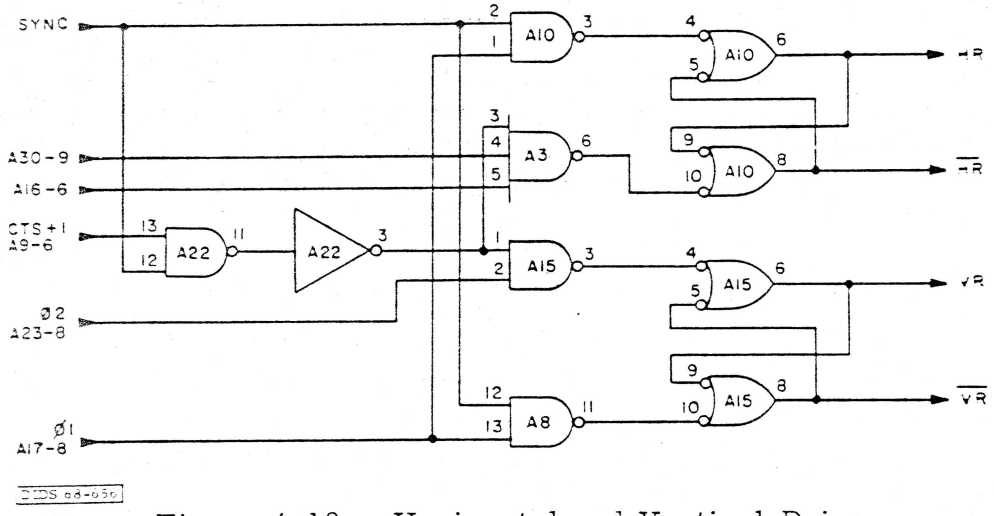


Figure 4-18. Horizontal and Vertical Drive

The horizontal retrace flip-flop A10-6 and A10-8 is set when gate A10-3 detects coincidence between Ø1 and the horizontal retrace pulse on the sync line. The HR flip-flop is reset when gate A3-6 detects coincidence among CTS+1, the horizontal reset pulse on the sync line, and the phase counter is at a count of Ø3. The output of the horizontal retrace flip-flop is shown in figure 4-19.

4-8.5 Vertical Drive

The vertical drive circuit (also referred to as vertical retrace), shown in figure 4-18, is composed of a latch-type flip-flop A15-6 and A15-8. The output from the vertical retrace (VR) flip-flop (figure 4-19) is a gate approximately 1152 μs wide, which represents the vertical retrace time and is equivalent to one horizontal line time. The gates are 14.948 ms apart: this represents the frame time, or the time taken to generate 12 horizontal lines plus the VR time. The frame rate is 67 Hz, the rate at which each character circulates through the memory loop.

The VR flip-flop A15-6 and A15-8 is set when gate A15-3 detects coincidence between CTS+1, Ø2 and the horizontal-vertical retrace pulse on the sync line. This flip-flop is reset when gate A8-11 detects coincidence between Ø1 and the horizontal retrace pulse on the sync line.

4-8.6 First and Last Word of Line

The first and last word of line circuits, shown in figure 4-20 are composed of A18-6, and A18-8. The FWL pulse indicates that the first character of a line is about to enter the entry register. The LWL pulse indicates that the last active character (character 42) is about to enter the entry register.

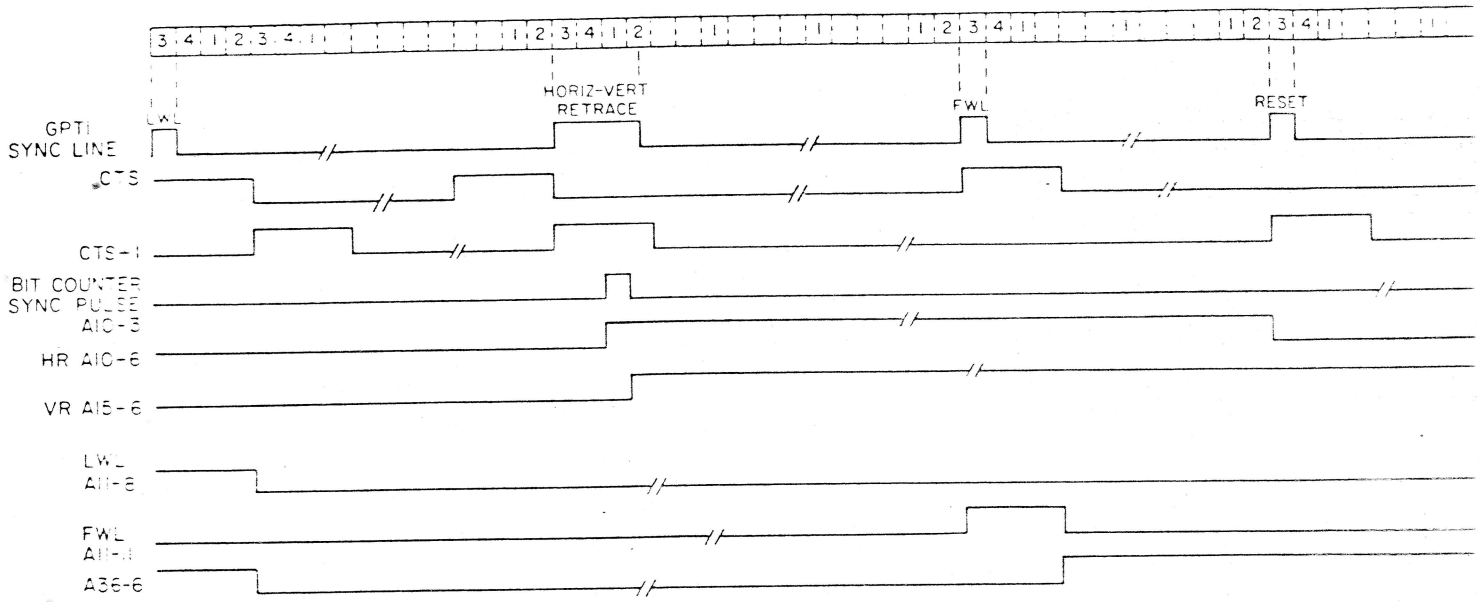
The FWL pulse is developed in gate A18-6 with the combination of HR, $\overline{\text{SYNC}}$, and CTS. The signal is then inverted and presented at A11-11 as FWL. LWL is developed in gate A18-8 with the combination of CTS, $\overline{\text{SYNC}}$, and $\overline{\text{HR}}$. The signal is then inverted at A11-8. The outputs of these two gates are shown in figure 4-19.

4-8.7 FΔ (First character, first line)

The FΔ circuit shown in figure 4-21 is composed of a differentiator, circuit and NAND-gate A44-11. The $\overline{\text{VR}}$ pulse from A15-8 is applied through inverter A44-6 to the differentiating circuit where it is applied as a positive going pulse at NAND gate A44-13. When this pulse occurs in coincidence with the FWL signal, an FΔ signal is developed at A44-11 and inverted in inverter A44-8.

4-8.8 Blanking

The output of blanking circuit A3-8 is used to cut off the video amplifier during the inactive scan periods of the monoscope and CRT. The most frequent blanking level occurs once per character during CTS+1 which is applied to A3-11. This pulse is used to cut off the video amplifier while the monoscope beam is being directed to the next character symbol to be displayed. The next most frequent blanking signal (assuming a full screen display) is the $\overline{\text{HR}}$ signal, which is applied to A3-9. This level is six characters wide and occurs during horizontal retrace. This in turn cuts off the video amplifier during retrace to protect the CRT screen phosphor.


LWL
HORIZ-VERT RETRACE
FWL
RESET
GPTI SYNC LINE
CTS
CTS-1
BIT COUNTER SYNC PULSE
AIC-3
HR AIC-6
VR AI5-6
LWL AII-8
FWL AII-8
A36-6

DIDS 66-155

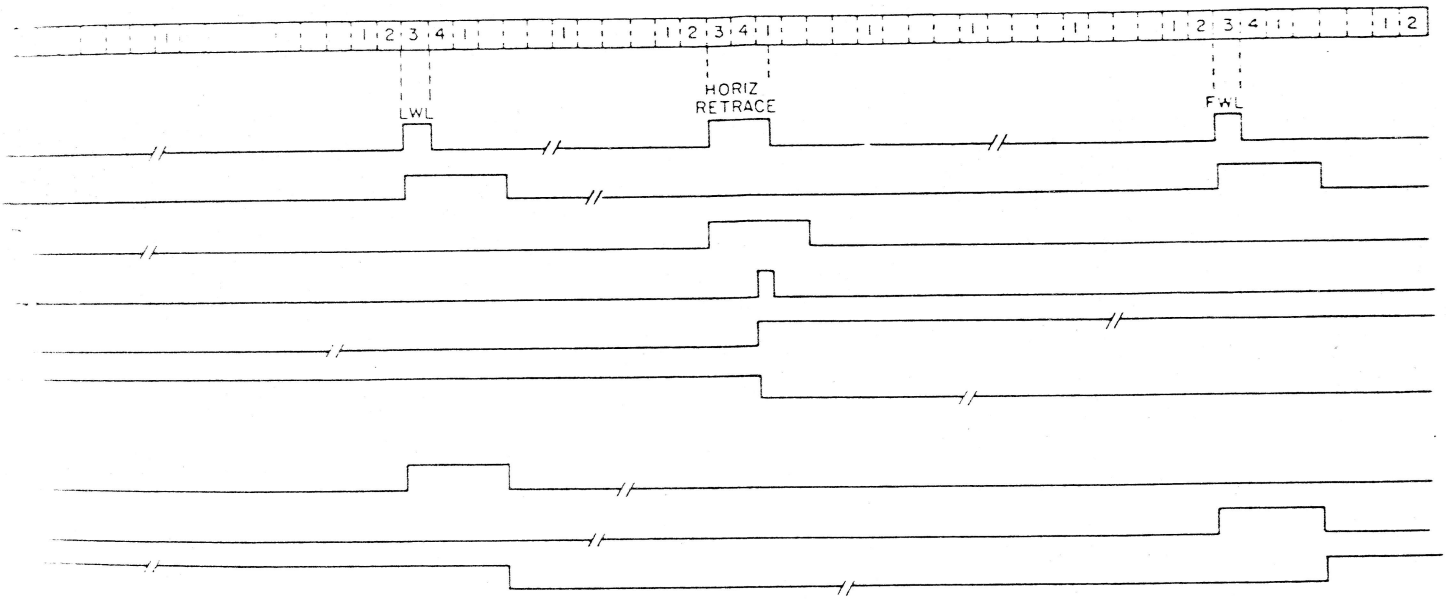


Figure 4-19. System Timing

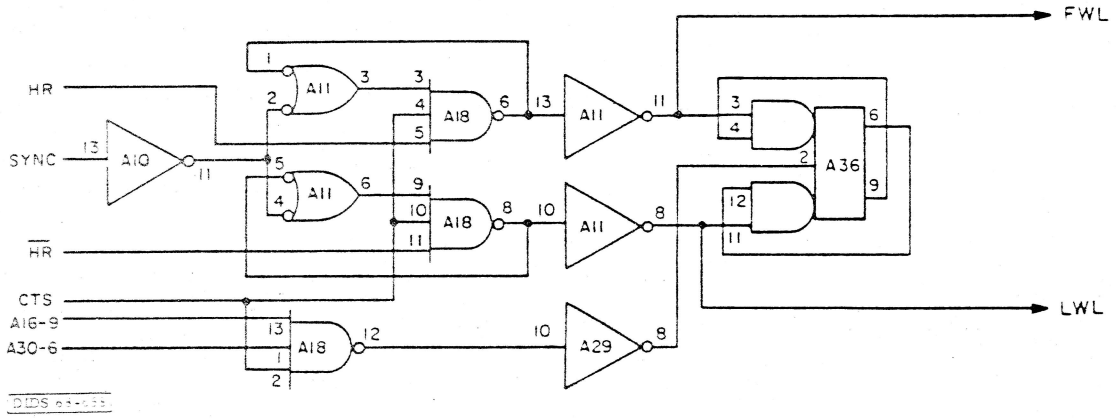


Figure 4-20. First and Last Word of Line

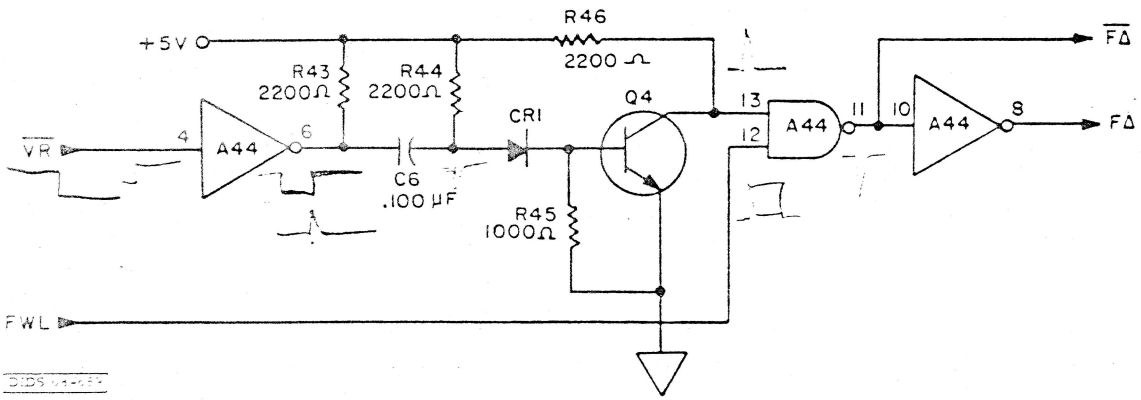


Figure 4-21. FΔ Pulse

The $\overline{VR}$ blanking level operates in a similar manner but is present for 48 character times. The $\overline{VR}$ pulse (which is immediately followed by $\overline{HR}$) cuts off the video amplifier once per frame to protect the CRT phosphor during vertical retrace.

4-8.9 6 Hz Oscillator

See Figure 7-16 (Raytheon Drawing 345405). The 6 Hz oscillator is a freerunning multivibrator. One transistor conducts while the other is cut off. When the conducting transistor reaches saturation there is no further change in current and its collector capacitor begins to discharge. This capacitor discharging brings the transistor which was cut off into conduction, cutting off the saturated transistor. Thus the two transistors cut off and conduct at a 6 Hz rate.

Diodes CR13 and CR2 are used to inhibit the 6 Hz oscillator during transfer of data between the display terminal and the GPTI.

4-9 Display Editing

4-9.1 Character Entry Register

The character entry register (CE register), shown earlier in figure 4-5, consists of six data flip-flops and a cursor flip-flop. Data enter the character entry register from one of two different sources: the delay line, or the keyboard. The source of input data is dependent on the operating status of the display terminal at any particular moment.

4-9.1.1 Data From Delay Line. The CE register, as part of the refresh memory loop, accepts data characters from the delay line, causes the character to be displayed on the screen, and then returns the character to the delay line. The delay line is an internal storage device that provides a 14.948 ms delay of data between input and output. Since the CE register is connected in series with the delay line to form a loop, one character is

always present in the CE register for display. When a complete character has been shifted into the CE register, a pulse enables the character code to be parallel transferred into the character readout register (CR register) for displaying a corresponding visual character on the CRT screen.

Data characters circulating in the refresh memory consist of seven bits. These seven bits contain six data bit positions that are used to carry character code information while the seventh bit position is reserved for the cursor. When the cursor is attached to a character code, the cursor bit position contains a one. The cursor bit is movable and can only be attached to one of the 504 data characters or 120 retrace characters held in the delay line.

Data from the delay line enters the CE register at the input to register flip-flop A69-6 (see figure 7-16, Raytheon Drawing 345405) after having passed through the output display logic. Phase two clock pulses are constantly applied to the CE register; thus, an uninterrupted stream of serial data is constantly circulating through the register. Since data are transferred LSB first, the cursor bit position is the first portion of a character to enter the register. This bit will be clocked into A69-6 during CTS+1. The next six successive Ø2 pulses shift the character into the register until, after seven bit times, a complete character is held in the register. It is at the end of CTS time that the character code is parallel transferred into the character readout register.

Data leaves the CE register from the set output of A70-6 and is coupled to the delay line via input display logic. After a character enters the delay line, it will be returned to the CE register after a delay of 14.948 ms. This time interval corresponds to the frame time, or the time required for the CRT scan to leave a particular position on the screen, move through an entire scan of the screen, and return to the original position on the screen. Since the character code will once again be transferred to the CR register, the visual character displayed on the CRT screen will be "refreshed."

4-9.1.2 Data From Keyboard. The CE register enables display terminal operators to enter keyboard information into the refresh memory loop. Each time the operator depresses any character key, a six bit digital code and a strobe pulse are produced. The six bit code is peculiar to the particular key depressed and the strobe pulse is present each and every time a character key is depressed.

Assuming that the "A" key is depressed, the code present at the inputs to the strobe gates is 100001. This code is developed by a diode matrix located in the keyboard and is illustrated in figure 4-3. This code will be present at the input to each gate for as long as the key is held depressed (usually 20 to 50 ms).

The strobe input to the circuits shown in figure 4-22 is normally high. The depression of any character key causes a high to low level change on the strobe line. When the A key is depressed a low level is applied to input gate A78-10 of the sample strobe flip-flop A62-6. The low level is also applied through inverter A65-3 to the input gate (A65-11) of the strobe flip-flop, A60-8. The sample strobe flip-flop is normally held in the zero state thereby allowing all FΔ and $\overline{F\Delta}$ pulses to be coupled through gates A60-11 and A60-3, respectively. Upon receipt of the first FΔ pulse after the key has been depressed, the sample strobe flip-flop is set to the one state blocking any further FΔ pulses from passing through gates A60-11 and A60-3. The sample strobe flip-flop will continue to inhibit any pulses from passing through the gates until the key is released by the operator, at which time the sample strobe flip-flop will be cleared to the zero state. The first FΔ pulse after the key is depressed is applied to gate A65-13 in coincidence with the strobe pulse which together set the strobe flip-flop, A60-8, and the step-right flip-flop, A67-12. The strobe flip-flop and the step-right flip-flop will remain set until the cursor is detected in the cursor flip-flop of the CE register.

The cursor, which is attached to the LSB of one character in memory, will be shifted into the CE register from 0 to 14.948 ms after the key is

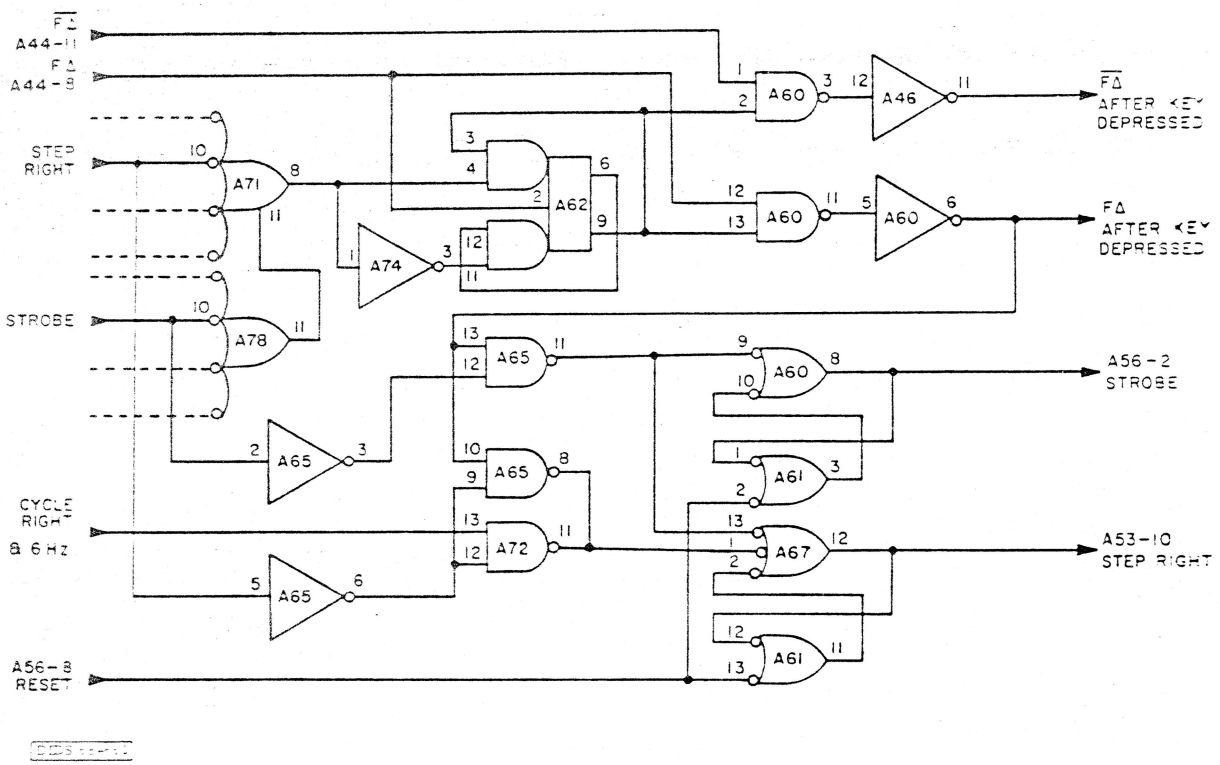


Figure 4-22. Strobe Circuits

depressed. When the character containing the cursor is shifted into the CE register, the cursor locate gate A46-6 will produce a pulse which is applied to gates A56-12 and A53-8 (see figure 7-16, Raytheon Drawing 345405).

The output of gate A56-12 is a pulse one CTS wide, and is used to clear the CE register and then shift in the keyboard data. The output of A56-12 is applied to the clear pulse gate A45-6 and the write pulse gate A52-12. Gate A45-6 detects coincidence between CTS time and Ø3. If this coincidence takes place during a displayable portion of a line, as determined by gate A22-6, a clear pulse is produced which is applied to the jam clear inputs of the CE register. Next gate A52-12 detects coincidence between CTS and Ø1. If this coincidence occurs at any time other than at a retrace time, as determined in flip-flop A51-6, a pulse is developed which allows the keyboard data to enter the CE register.

At the same time that data are being transferred into the CE register, gate A53-8 develops a pulse that is applied to gate A56-8 which in turn resets both the strobe flip-flop and the step-right flip-flop. The output pulse of A53-8 is also used to advance the cursor by one character. This is accomplished by applying a low signal to A57-12 which places a high level at the input to the CE register. At the input of the CE register is the CTS bit of the next character; therefore, the cursor is shifted right one character. The cursor is removed from the character in the CE register by placing a low at A57-5, which places a low level in the bit now entering the delay line from the CE register. This bit is the CTS time of the character now in the CE register; therefore, the cursor is removed.

It should be noted that if a character code is associated with the cursor, the code is cleared before entering a new character from the keyboard. This accounts for the destructive effect of positioning the cursor over a character and then depressing a character key. A timing diagram illustrating the keyboard entry process is shown in figure 4-23. As explained in the previous text, four separate actions occur almost simultaneously. These actions are: 1) clear CE register; 2) strobe digital code into CE register; 3) step the cursor right one character position; and 4) reset flip-flops.

4-9.1.3 Decode. The CE register and gates A71-6 and A78-4 (see figure 7-16, Raytheon Drawing 345405) are responsible for detecting when a carriage return code is present in the CE register. When the carriage return code (111101) is detected a signal is sent to the advance line function.

4-9.2 Character Readout Register

The character readout (CR) register is a part of the character generation circuitry. Character codes are entered into the CR register from the CE register and held for one character time (from CTS to CTS). During this time, the monoscope beam is deflected to a specific character position on the monoscope front to produce a visual character on the CRT screen. The important fact to remember about the CR register is that the digital code

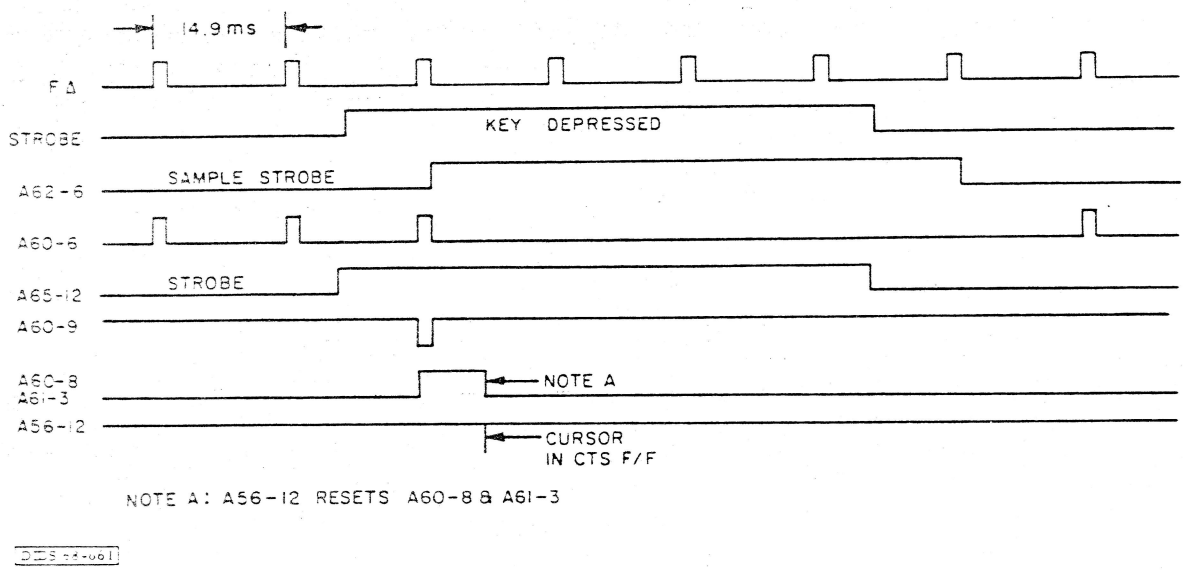


Figure 4-23. Data Entry Timing Diagram

held in the register determines which of 58 individual visual characters will be displayed on the screen. (See figure 4-5.)

When a character code is entered into the CE register from any of the input sources, a complete seven bit code will be available for transfer during CTS. The code is coupled from the one and zero side output of each CE register flip-flop and applied in parallel to the inputs of each flip-flop of the CR register. During CTS, the digital code held in the CE register is clocked into the CR register. From the CR register, the six bit code is divided into two three-bit segments. These segments are coupled to the monoscope deflection amplifier and direct the monoscope beam to a specific character on the monoscope target. The CR register also contains a cursor flip-flop, A35-6. The output of the cursor flip-flop is applied to the write cursor line.

4-9.3 Display Functions

In addition to enabling the generation of visual characters on the CRT screen, circuits contained on the display logic board enable various edit and cursor control functions to be performed. These functions are listed below and described in the following text:

- Step Right
- Cycle Right
- Step Left
- Cycle Left
- Step Up
- Step Down
- Carriage Return
- Frame Reset
- Screen Erase

4-9.3.1 Step Right Function. The step right function shown in figure 4-22 (also see figure 7-16, Raytheon Drawing 345405) moves the cursor one character position to the right. The visible effect of step right is to move the cursor (⌟) one character position further from the left side of the CRT screen. In memory, step right causes the cursor to appear in the CE register 24 μs later than it had prior to the step right function.

The step right function is performed each time one of the following occurs:

- The step right ([→]) key is depressed.
- Any key capable of producing a digital code is depressed and data are entered into memory.

To perform a step right function, the cursor is located in memory by the cursor locate gate A46-6 (figure 7-16, Raytheon Drawing 345405), sensing the cursor in cursor flip-flop A70-6 of the CE register. When the cursor is found, it is erased and then reinserted into memory at the entrance to the

CE register. The combined effect of these two operations is to delay the cursor by one character time. The step right function is described in the following text.

When the step right (⇥) key is depressed, a high to low level change takes place on the step right line. This low level is applied through an inverter to the step right input gate A65-9. The low level is also applied to the sample strobe input gate A71-10 which sets the sample strobe flip-flop A62-6 blocking any further FΔ pulses from passing through gate A60-11. The last FΔ pulse to pass through gate A60-11 after a key has been depressed is applied to A65-10 which in turn sets the step right flip-flop, A67-12.

The step right flip-flop can also be set by a strobe pulse which is produced in gate A65-11 when a character key is depressed.

With the step right flip-flop set, gate A46-6 (figure 7-16, Raytheon Drawing 345405) searches for the cursor bit. When the cursor bit appears in the cursor flip-flop of the CE register, gate A46-6 applies a pulse one CTS wide to gate A53-9. The output of A53-8 then goes low. This low is applied to cursor erase gate A57-6 where the cursor is removed from the data now entering the delay line. This low signal from gate A53-8 is also applied to cursor enter gate A57-11 where a high is applied to the input of the CE register in coincidence with the CTS of the next character.

The step right circuit is used to move the cursor to the right each time a character is depressed. If a character is entered during the last character of a line, the step right circuit is made to step the cursor right automatically until the first character of the next line. The manner in which this is accomplished is explained below.

When a character is entered from the keyboard during the last character of a line, the strobe flip-flop and the step right flip-flop are set exactly as they were during any character entry. The following steps occur in order.

1. As soon as the cursor is detected in the cursor flip-flop, gate A57-11 inserts the cursor at the entrance of the CE register. At the same time the cursor is removed by gate A57-6 from the character now leaving the CE register. The cursor has now been moved right to the next character.

2. During Ø3 of the cursor bit the clear pulse is produced which jam clears the CE register. This clear pulse is generated in gate A45-6.

3. During Ø1 of the cursor bit, the character code of the key depressed is strobed into the CE register.

4. The advance line flip-flop A51-8 is set by gate A45-8's detecting coincidence between the cursor bit, Ø2, LWL, and the step right flip-flop being set. The advance line flip-flop will remain set until the FWL pulse and Ø1 are detected by gate A9-8. When the advance line flip-flop is set, no write pulses are produced. The advance line flip-flop also applies a low level to the function reset circuit. This low level takes the place of the low level previously applied by the step right circuit.

NOTE

The function reset circuit is a differentiator; therefore, the signal applied to this circuit at gate A56-8 must go low, and then high again. The function reset pulse is produced when the input signal goes from a low level to a high level. It is for this reason that the low input to this circuit must be removed before the step right circuit can be reset.

Because the step right flip-flop has not been reset, gate A53-8 will continue to step the cursor right each time it is detected in the CE register. The cursor will continue to be stepped right until the FWL pulse in coincidence with the Ø1 signal resets the advance line flip-flop. When this flip-flop is reset, the low level is removed from the function reset circuit and a reset pulse is produced. The reset pulse resets the step right flip-flop, thereby ending this function.

4-9.3.2 Cycle Right Function. The cycle right function is initiated when the step right key is fully depressed. The operation of the cycle right function is identical to that of the step right function with the only exception that the operation is repeated at a 6 Hz rate.

The 6 Hz oscillator is continually applying its signal to A72-13 (figure 7-16). This 6 Hz signal is blocked by gate A72-3 when the cycle mode is not used. This is accomplished when both inputs to gate A72-3 are high, which will be the case when not in a cycle mode. When both inputs are high the output will be low or at ground level. It is this ground level that blocks the 6 Hz output.

When the cycle mode is initiated, the output of A72-3 goes high, therefore allowing the 6 Hz signal to be applied to gate A72-13. The signal is then coupled through gate A72-11 where it sets the step right flip-flop at a 6 Hz rate until the key is released. Note that the 6 Hz signal takes the place of the FΔ pulse which was previously used to set the flip-flop.

4-9.3.3 Step Left Function. The step left cursor control function moves the cursor one character position to the left. The visible effect of step left is to move the cursor one character position closer to the left side of the CRT screen. In memory, step left advances the cursor by one character time, causing it to appear in the CE register 24 μs earlier than it had prior to the step left function. See figure 4-24.

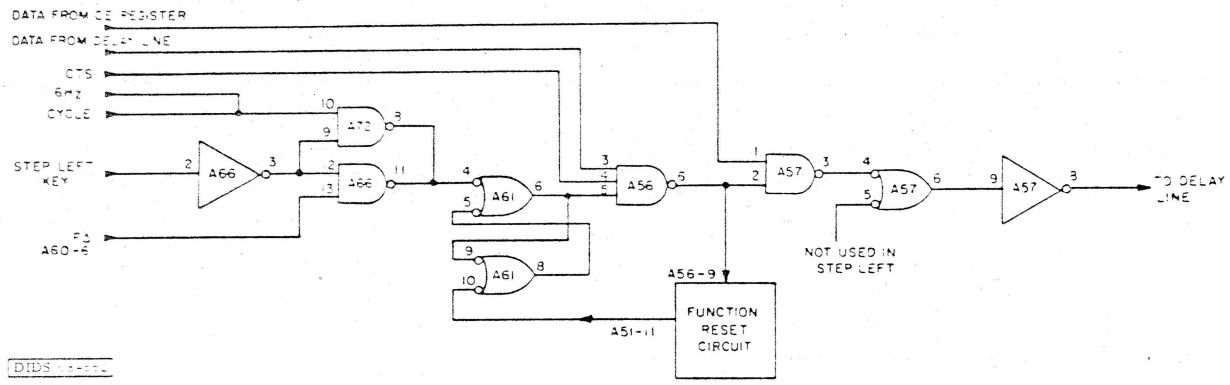


Figure 4-24. Step Left and Cycle Left Logic Diagram

The step left function is performed each time the step left (←) key is depressed. To perform a step left function, the cursor is located in memory by examining the output of the delay line during CTS. (Remember that the cursor is the only bit in memory that is high during CTS.) Once located, the cursor is erased prior to entering the CE register and inserted at the output of the CE register. In essence, the cursor bypasses the shifting through the CE register. The time saved in this manner allows the cursor to appear 24 μs earlier than it had previously.

When the step left key (←) is depressed, a high to low level is applied through an inverter to the step left input gates A66-11 and A72-8. Gate A72-8 is used only during a cycle mode and will be discussed later. The high to low level on the step left input line is also applied to the sample strobe circuit where the last FΔ pulse after a key is depressed is allowed to pass.

The FΔ pulse in coincidence with the step left signal sets the step left flip-flop, A61-6. Gate A56-6 is used to detect the cursor leaving the delay line. When the cursor is detected it is erased from the character with which it was associated. The low level that was placed in the CTS time slot by gate A56-6 is combined with the CTS bit of the character now leaving the CE register. This combination takes place in gate A57-3 which places a high level in the CTS of the character to the left of the original character. This is illustrated in figure 4-25.

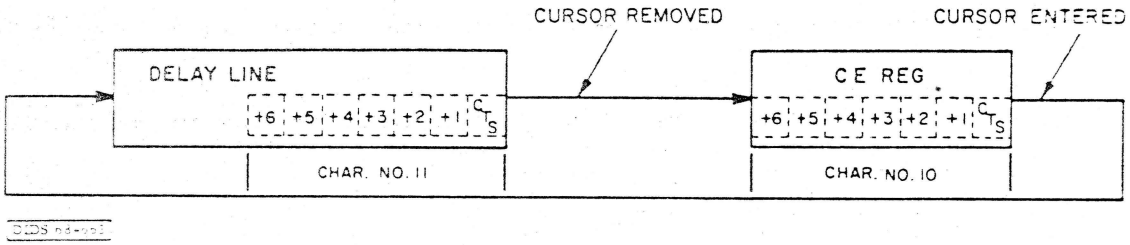


Figure 4-25. Step Left (Cursor Removed and Entered)

4-9.3.4 Cycle Left Function. The cycle left function is initiated when the step left key is fully depressed. The operation of the cycle left function is identical to that of the step left function with the only exception that the operation is repeated at a 6 Hz rate.

The 6 Hz oscillator is continually applying its signal to A72-10. This 6 Hz signal is blocked by gate A72-3 when the cycle mode is not used. This is accomplished when both inputs to gate A72-3 are high. When both inputs are high the output will be low or at ground level. It is this ground level that holds the 6 Hz output at ground.

When the cycle mode is initiated the output of A72-3 goes high, allowing the 6 Hz signal to be applied to gate A72-10. The signal is then coupled through gate A72-8 where it sets the step left flip-flop at a 6 Hz rate until the key is released.

4-9.3.5 Step Down. The step down cursor control function moves the cursor from any character position of a line to the same character position of the next line. In memory, step down consists of delaying the cursor by 48 character times (one line time) and causing it to appear in the CE register 1152 μs later than it had prior to the initiation of the function.

To perform a step down function, the cursor is located in memory by sensing its presence in the cursor flip-flop of the CE register. When the cursor is found, it is erased and then reinserted into memory after counting 48 characters. This delays the cursor by 1152 μs and places it on the next

horizontal line immediately under where it was prior to the function. See figure 7-16, Raytheon Drawing 345405.

When the step down key (↓) is depressed, a high to low level change takes place on the step down line. This level change is applied to step down input gate A79-11 through an inverter A79-3. The level change is also applied to the sample strobe circuit where an FΔ pulse is allowed to enable gate A79-11, setting the step-down flip-flop A79-6.

The next step in making the cursor move down one line is to enable the character counter to begin to count. To see how this is accomplished, see figure 4-26.

The character counter is disabled by the jam clear inputs until a signal is received from either the step up circuit or the step down circuit. Flip-flop A47-6 determines when the character counter and the line counter will be allowed to count. For either of these two counters to count, the signal at the jam clear input must be removed, at which time the counters will begin to count.

When step down flip-flop A79-6 (figure 7-16, Raytheon Drawing 345405) is set, a low level output will be produced in the second half of step down flip flop A79-8. This signal is applied to A80-6 which in turn satisfied one input of line tag flip-flop A47-6. This signal is also applied to gate A53-6 which will remove the cursor when it is detected in the cursor flip-flop of the CE register.

When the cursor is detected by cursor locate gate A46-6 a high level is applied to both the cursor removal gate, A53-6, and the flip-flop, A47-6. Immediately upon detection of the cursor, gate A53-6 produces a low output which removes the cursor from the data now leaving the CE register. Flip-flop A47-6 is triggered on a Ø2 pulse; therefore, the flip-flop will be set at the end of the CTS time. Once flip-flop A47-6 is set, the jam clear inputs to the character counter are removed and the counter begins to count. The

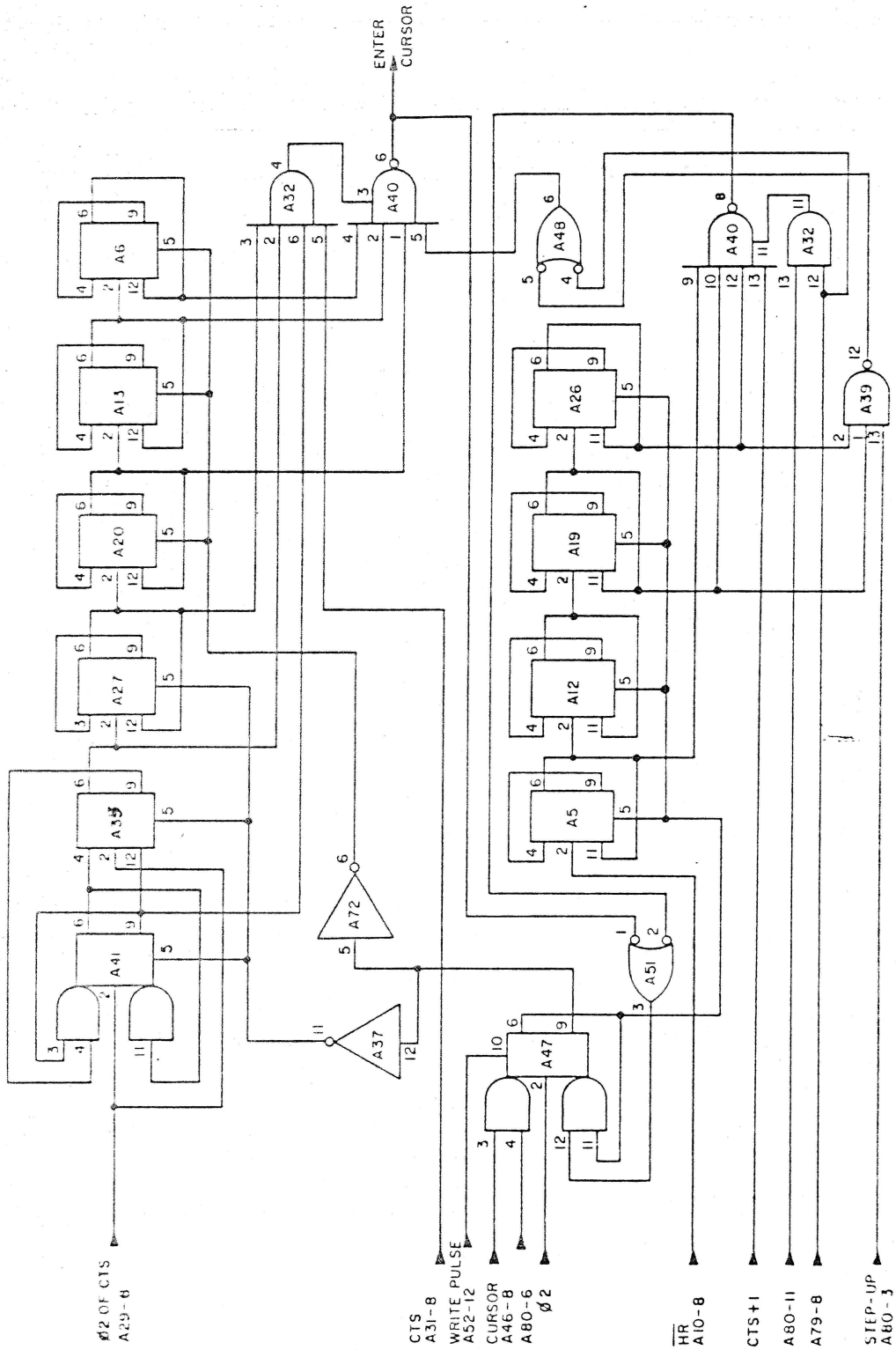


Figure 4-26. Line Counter and Character Counter

counter is made up of six flip-flops (figure 4-26). The counter is triggered during each Ø2 of CTS time. The various stages of the counter are shown in figure 4-27.

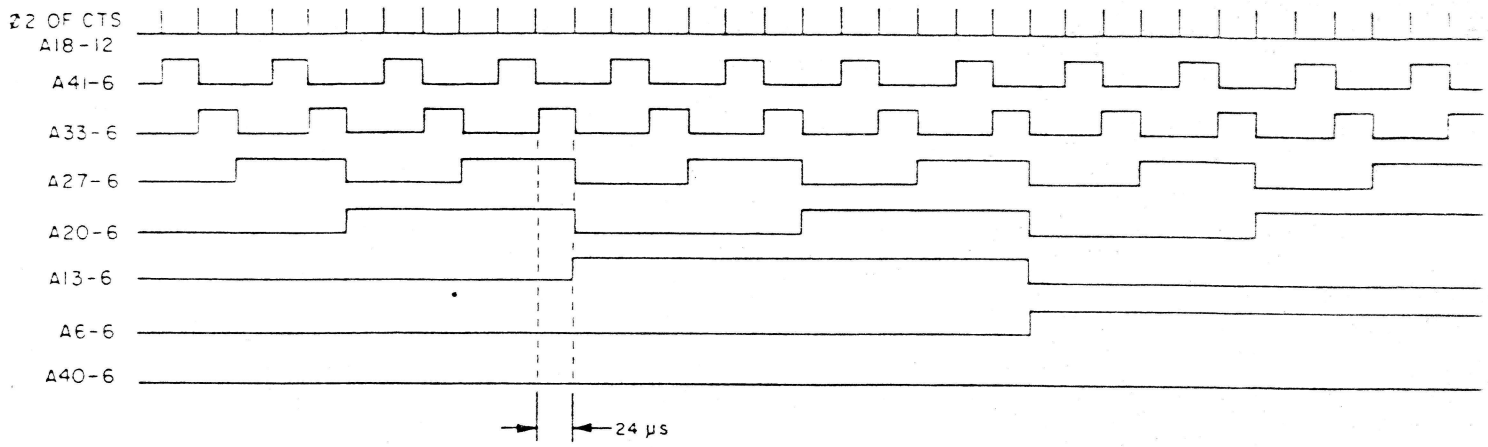
Gate A40-6 is used to decode a count of 48 characters. Gate A48-6 is used to determine whether the decode should be made after one line or after 12 lines. When the decode is made after 48 characters, a low level is developed by gate A40-6 which is applied to gate A57-3. Gate A57-3 is used to add the cursor to the data now entering the delay line. The cursor was placed in the same character position as before but was delayed by one line.

The decode signal which was made after a 48 character count is also applied through gate A51-3 to the input of flip-flop A47-6. At the next Ø2 after decode the flip-flop is reset, reapplying the jam input to both the character counter and line counter.

The decode signal is also applied to the function reset circuit, which in turn resets the step down flip-flop. Once the step down flip-flop has been reset, the step down function is complete.

4-9.3.6 Step Up. The step up cursor control function moves the cursor from any character position of a line to the same character position of the previous line. In memory step up causes the cursor to appear in the CE register 13.824 ms later than it had prior to initiating the step up function. This 13.824 ms delay represents one frame time minus 48 character times (14.976 ms - 1.152 ms = 13.824 ms). After the cursor is delayed by 13.824 ms, it is reinserted into the delay line to accomplish the step up function.

The step up function is accomplished by employing two counters; the character counter and line counter. The line counter output is used to delay the cursor by 12 line times. The character counter, which starts counting at the cursor location, counts until a count of 48 is obtained. Each time the character counter completes counting 48 characters, it immediately starts to count again until the line counter decodes twelve lines. The counter


Ø2 OF CTS
A18-12
A41-6
A33-6
A27-6
A20-6
A13-6
A6-6
A40-6
24 µs

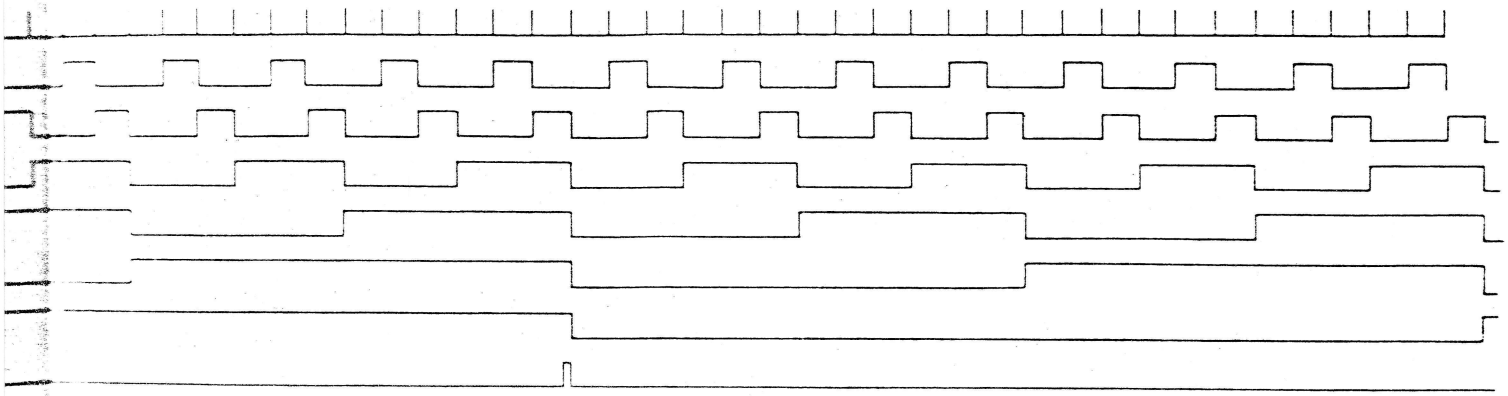


Figura 4-27. Representación de los Tiempos del Contador de Caracteres

continues in this manner until the line counter counts 12 lines, followed by the character counter counting 48 characters. These two outputs combined represent a total delay of 13.824 ms and enable placing of the cursor immediately above the cursor position of the previous line.

When the step up key is depressed, the sample strobe circuit generates a FΔ pulse which is applied to step up input gate A66-8 (figure 7-16), Raytheon Drawing 345405). When this pulse occurs in coincidence with the high level on the step up line, gate A66-8 produces a pulse which sets the step up flip-flop A80-3. When the step up flip-flop is set gate A80-6 applies a high to both gate A53-6 and flip-flop A47-6.

When the cursor is detected in the CTS flip-flop of the CE register, cursor locate gate A46-6 produces a pulse which is applied to gate A53-6 and flip-flop A47-6. When this pulse is applied to A53-6, the cursor is removed from the character in the CE register. This cursor locate pulse, in coincidence with a Ø2 trigger pulse, sets flip-flop A47.6. Once this flip-flop is set, the jam inputs are removed from the counters and they are allowed to count.

The character counter counts in the same manner as it did in the step down function. The decode which counts 48 characters is blocked at A40-5 until the line counter has counted 12 complete lines.

The line counter (figure 4-26) is held in the jam clear state until either the step up or step down keys are pressed. Once the jam is removed the counter is triggered on each $\overline{HR}$ pulse. The twelfth line is decoded in gate A39-12 which then allows the character counter decode to be developed in gate A40-6.

When the decode is produced it is applied to gate A57-3 which places the cursor in the CTS of the character now entering the delay line. The decode is also used to reset flip-flop A47-6. When A47-6 is reset the jam signals are once again applied to the counters disabling each of them. The decode

is also used by the function reset circuit to reset the step up flip-flop. Once the step up flip-flop has been reset the step up function is complete.

4-9.3.7 Frame Reset. The frame reset function moves the cursor from wherever it appears on the CRT screen to the frame reset (first character first line) position. In memory this amounts to placing a low at the input to the CE register during every CTS except FΔ. This in turn assures that wherever the cursor appears in memory it will be erased. When the CRT scan is at the frame reset position, FΔ is gated through to enter the cursor at that position.

When the frame reset key is depressed, gate A39-6 (figure 4-28) will apply a high to gate A39-8 and A38-3. Other inputs to gate A39-8 include CTS and FΔ. The FΔ signal is normally high and goes low only during the first character of the first line. Therefore, during each CTS pulse except FΔ, gate A39-8 produces a low pulse output which ensures that any cursor in the memory loop will be erased as it enters the CE register.

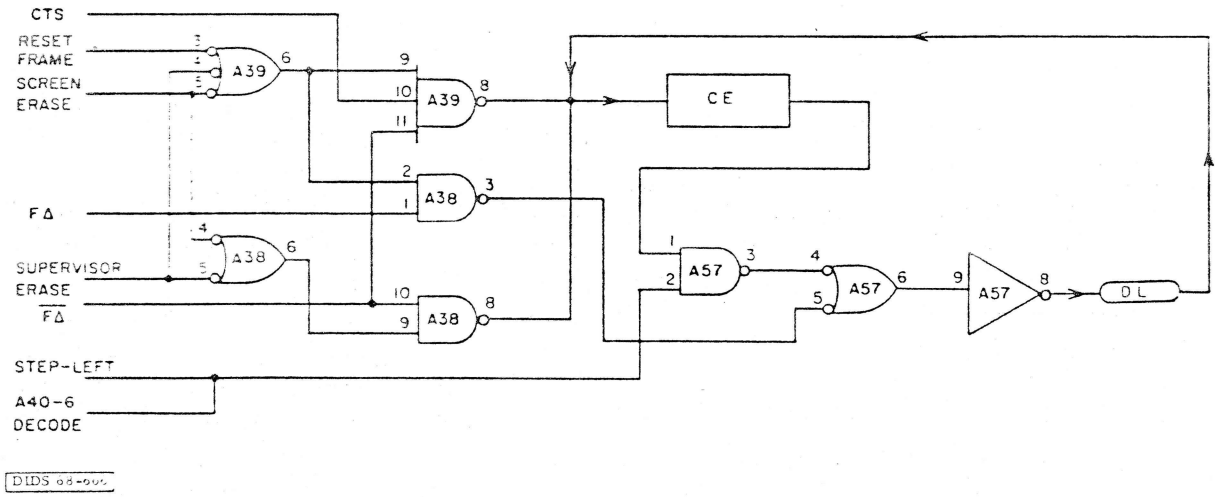


Figure 4-28. Screen Erase and Frame Reset

Gate A38-3 is used to enter the cursor during FΔ. The inputs to this gate are the frame reset signal and the FΔ pulse. Therfore, during FΔ time gate A38-3 produces a low pulse out which is applied to gate A57-6 and A57-11. Gate A57-6 uses this pulse to ensure that there is no cursor in the character now leaving the CE register. Gate A57-11 is used to insert the cursor in the character now entering the CE register. This function is completed when the operation releases the frame reset key.

4-9.3.8 Screen Erase. The screen erase function, figure 4-28, is used to erase all characters in the memory loop from the FΔ position to the end of the frame. In memory, the screen erase function inserts all "0's" in each character bit. When the screen erase key is depressed a low level is applied to gates A39-6 and A38-6. From gate A39-6 on, the circuit functions in the same manner as it did during a frame reset function.

Gate A38-6 produces a high level output for as long as the screen erase key is depressed. This high is applied to gate A38-8 along with FΔ pulse. The output of A38-8 is low for all character times except FΔ time. This low level output is applied directly to the input of the CE register, thereby erasing all characters as they are about to enter the CE register. During the first character of the first line the erase signal produced in gate A38-8 is removed, thereby allowing the cursor to be entered at FΔ time. The screen erase function is completed when the screen erase key is released.

4-9.3.9 Carriage Return. The carriage return function is performed each time the operator depresses the carriage return key (⏎). To perform the carriage return function the cursor is delayed in time until the first character slot of the next horizontal line. To accomplish this, the cursor right circuit is made to operate continually until the first character of the next horizontal line. During the time that the cursor right circuit is operating, the cursor symbol cannot be seen when it moves across the CRT. All characters to the right of the carriage return are erased.

When the carriage return key is depressed a six bit digital code is developed in the keyboard matrix. This code (111101) is applied to the strobe input gates of the CE register. The carriage return code is now entered into the memory in the same manner as any other character code. Immediately after the carriage return code is parallel shifted into the CE register, gate A71-6 makes a carriage return decode. This decode takes place during Ø2 of CTS time. This decode sets the advance flip-flop A51-8. As soon as the advance line flip-flop is set, the write cursor circuit is disabled so that the cursor cannot be seen moving across the screen. The advance line flip-flop holds the input to the function reset circuit low, thereby blocking any function reset pulse. The advance line output is also applied through gate A53-3 to the clear pulse gate A45-6. The write pulse gate A52-12 is disabled by this output; therefore, no characters will be strobed into the CE register while the advance line flip-flop is set. The clear pulse gate will jam clear the CE register each time the cursor is detected in the cursor flip-flop of the CE register. Remember that since the step right circuit was not reset the cursor will automatically be stepped right until the advance line flip-flop is reset. Because the cursor automatically shifts to the right and the clear pulse gate jam clears the CE register each time the cursor appears, any character that appeared on the same line but to the right of the carriage return (⏎) is erased.

The carriage return function is terminated when the advance flip-flop is reset by gate A9-8 detecting Ø1 of the FWL pulse. Upon resetting the advance line flip-flop, the function reset circuit produces a pulse which resets the step right flip-flop. The cursor is now positioned at the first character of the next line.

4-9.3.10 Line Tag. The line tag circuit utilizes the same circuits as did the line counter circuit, with the exception that a new decode circuit is used. A line tag, which is a logic one in the LSB of the first horizontal retrace character, is placed at the start of each line that contains data. This line tag is used by the GPTI to determine which lines contain data and which lines are blank. The manner in which line tags are inserted is described as follows.

A write pulse is produced by gate A52-12 (figure 7-16, Raytheon Drawing 345405) each time a character is entered from the keyboard. This write pulse is used to "strobe" the character code into the CE register. This write pulse is also used to jam set flip-flop A47-6. As explained in previous discussions, when flip-flop A47-6 is set, the jam inputs are removed from both the character counter and the line counter. With the jam inputs removed both counters begin to count. When the line counter reaches the thirteenth horizontal retrace time and decode A40-8 detects CTS+1, a pulse is produced which is applied to both gate A81-8 and the input gate A51-3. The pulse, applied through gate A51-3 along with a Ø2 timing pulse, resets flip-flop A47-6 thereby reapplying the jam signal to the character and line counters. The output of decode gate A40-8 will be produced only if the step up and step down functions are not in effect. This decode output is applied along with Ø1, and the first character of horizontal retrace at gate A81-8, which in turn jam sets flip-flop A64-6 of the CE register. When jamming takes place the first character of horizontal retrace is present in the CE register; therefore, the LSB is set to a one. It only takes one character per line to generate a line tag, but it is important to remember that for every other character entered during the same line the complete line tag process is repeated.

4-10 Receive and Transmit

The display terminal is a half- duplex device designed to transmit and receive digital information, but not simultaneously. The following text explains the operation of the transmit and receive circuits.

4-10.1 Receive Circuit

When the GPTI has a message ready for transmission to a display terminal, it raises the message transfer line. This level is coupled through a line driver where it is applied to the following (see figure 4-29 and also 7-16, Raytheon Drawing 345405):

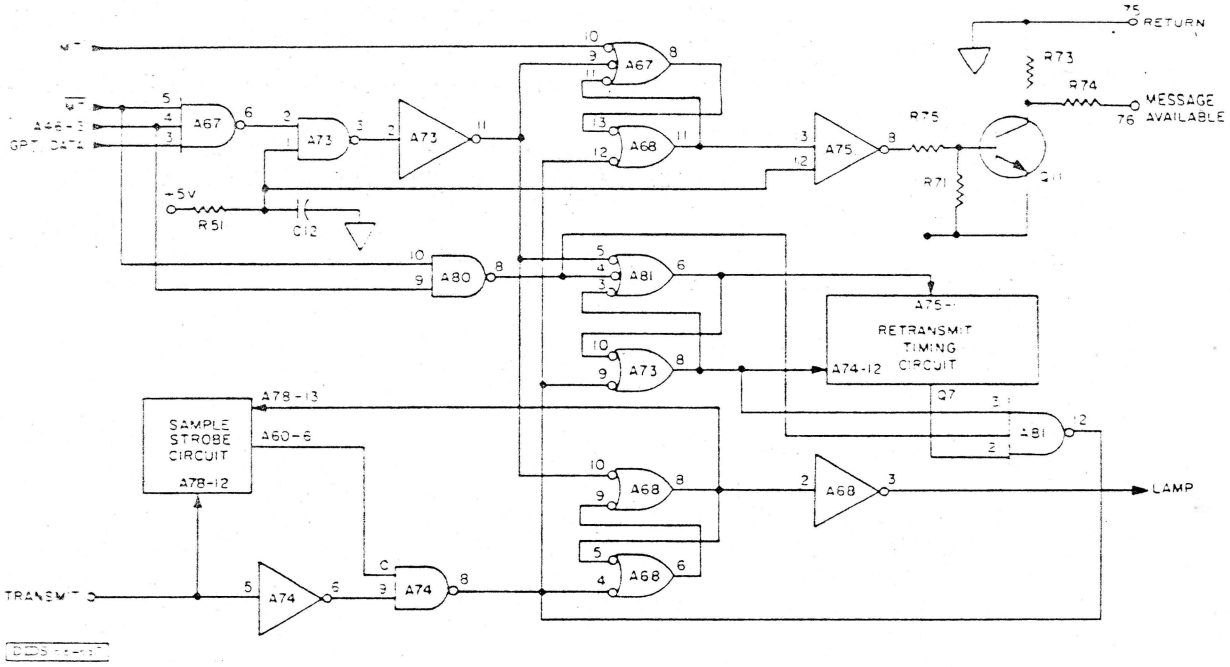


Figure 4-29. Receive and Transmit Circuit

a. Sample strobe circuit A71-9. The sample strobe circuit upon detecting the message transfer signal inhibits the keyboard.

b. Message available flip-flop A67-10. The message transfer signal ensures that the message available line is not "ON".

c. Delay line inhibit gate A52-8. The message transfer line when in the "ON" state inhibits any data leaving the delay line.

d. Data-in gate A52-6. The message transfer line must be "ON" in order for this gate to couple GPTI data into the memory loop.

Once the message available line is "ON", the GPTI will start data transfer as controlled by the GPTI program. The data are applied through gate A52-6 and A57-11 where they enter the CE register and then are shifted into the delay line. The location of the cursor is at the command of the GPTI and can be placed in any CTS.

The message transfer signal is removed when the GPTI completes the transfer of a message. When the message transfer signal is removed, data are once again allowed to pass from the delay line through the delay line inhibit gate A52-8, and into the CE register.

4-10.2 Transfer

Data transfer between the GPTI and the display is regulated by the GPTI. When the ENVIA (transmit) key is depressed, the key is illuminated indicating that a message is to be transferred to the GPTI, all keyboard functions are inhibited, and a signal is applied to the message available line which is sent to the GPTI.

When the GPTI is ready to receive data it "looks" to see what lines in the frame contain data. The lines which contain data have a line tag preceding the data. The line tag is placed in the first character of horizontal retrace. When the GPTI detects this line tag it starts to extract data from the delay line. When the GPTI has completed extracting data it generates an unlock code which is represented as a logic one during a horizontal retrace character. This unlock code is used to extinguish the ENVIA lamp and unlock the keyboard. This unlock code is also used to reset the retransmit timing circuit.

If the GPTI does not accept the data immediately, a timing circuit will generate a pulse that will keep the transmit mode active until the GPTI can accept the data. The transmit circuits function as follows.

When the operator depresses the ENVIA (transmit) key, a high to low level change takes place on the transmit line.

This low level is applied to the sample strobe circuit and through inverter A74-6 to gate A74-8. When the sample strobe circuit produces the last FΔ pulse after the key was depressed, gate A74-8 produces a pulse which sets the message available flip-flop, A68-11. The output of gate

A74-8 is also used to set flip-flop A68-6 which in turn illuminates the ENVIA key. Flip-flop A73-8 which is also set by this signal, allows the retransmit timing circuit to produce a pulse whose time is set by R62. Once the message available flip-flop is set the message available line is raised indicating to the GPTI that a message is ready for transmission.

When the GPTI is ready to accept data it extracts the data from the delay line by way of inverter A82-6. When the GPTI has accepted all the data, it generates an unlock code. This unlock code is a logic one during a retrace time. This unlock code is decoded in gate A67-6. Gate A67-6 generates a reset pulse when it detects coincidence among the unlock code, the first character of horizontal retrace, and the message transfer line "ON" condition.

This reset pulse is applied to flip-flop A68-8 which will extinguish the ENVIA light. The reset pulse is also applied to flip-flop A81-6 and A67-8 which turns off the retransmit timing circuit and resets the message available flip-flop.

4-10.3 Transmit Timing Circuit

The transmit timing circuit shown in Raytheon Drawing 345405 maintains the display terminal in the transmit mode until the GPTI has accepted the message. When the transmit key is depressed a high level is produced by flip-flop A73-8 which is inverted to a low level by A74-12. This low level allows Q9 to conduct. Flip-flop A81-6 also generates a low level which is inverted to a high by A75-6 and is applied to SCR, Q10. This positive on pin G of Q10 allows Q10 to conduct and appear as a short. With Q10 now conducting C18 begins to charge at a rate set by R62. When the potential on pin E of Q13 reaches the potential of pin B2 of the unijunction switch, Q13 will conduct allowing Q7 to produce a pulse which will maintain flip-flop A68-6, A73-8, and A68-11 in the transmit mode.

When an unlock code is received from the GPTI a pulse is generated which cuts off Q9 and blocks Q11, therefore inhibiting C18 from charging.

4-11 Delay Line Electronics A10

The delay line electronics board and the 14.948 ms delay line form a part of the refresh memory loop. The delay line, which has a total storage capacity of 624 characters, provides an economical means of storing data intended for display. Due to high delay line attenuation, read-write amplifiers are employed to amplify the data both before and after it is applied to the delay line section. See figure 7-14, Raytheon Drawing 343808.

Serial data enter the delay line electronics board at data-in terminals M and S. True data are applied to terminal S while the inverse of data is applied to terminal M. The data are clocked into the delay line electronics boards at A3-8 and A3-3 by a Ø4 clock which is applied to terminal T.

The true data are amplified by two amplifiers, Q6 and Q8, and then applied to input terminal R of the delay line. The inverted data are also amplified and applied to delay line input terminal N; Q5 and Q7 are used to amplify these data.

The data bit, now 0.857 μs wide (one phase time) appears at the output terminal of the delay line 7.474 ms later. The attenuated data reenter the delay line electronics at terminal B and are applied to the base of Q1. The attenuated data are amplified by Q1, Q2, and Q3 and applied to the base of Q4. The signal on both the collector and emitter of Q4 is amplified by Q9 and Q10 and applied to two flip-flops, A1 and A2.

Since the data bit is coincident with a Ø4 time, the bit will be entered into flip-flop A2. The reason for this is that A2 is toggled by a Ø4 signal, whereas A1 is toggled by a Ø2 signal. Once the bit has been entered in flip-flop A2 it is again applied to the input of the delay line electronics board at gates A3-11 and A3-6. Unlike the original data entry, this bit is entered during a Ø2 time. The Ø2 timing signal is applied to terminal V.

Once the bit has been reentered it is again delayed by another 7.474 ms and is reapplied to both flip-flops — A1 and A2. Since the data bit is now in coincidence with a Ø2 time, the bit is entered in flip-flop A1. Once entered in flip-flop A1, the bit is transferred out to the CE register with a total delay of 14.948 ms.

4-12 Monoscope Deflection Amplifier A3

The purpose of the monoscope deflection amplifier is to convert digital character codes arriving from the display logic board to analog deflection voltages. These analog voltages are then employed to position the monoscope scan to a corresponding character symbol on the monoscope target. In addition to positioning the scan, other signals developed on A3 cause the scan to sweep simultaneously up and down and across the character symbol (see figure 7-4, Raytheon Drawing 345409).

The monoscope deflection amplifier is composed of the following circuits:

- X and Y digital to analog converters
- X and Y deflection amplifiers
- X and Y skew correction
- minor vertical sweep generation
- unblanking pulse generation

4-12.1 X and Y Digital to Analog Converters

From previous discussions, the monoscope target is composed of 58 separate character symbols arranged in an eight-row eight-column coordinate system. The monoscope scan is directed to a particular column on the target by a Y axis deflection voltage. This voltage is developed by summing the binary values of the three MSB's of a character code held in the CR register. Conversely, the monoscope scan is directed to a particular row

on the target by an X axis deflection voltage. This voltage is developed by summing the three LSB's of a character code held in the CR register. The particular character being scanned at any given moment is determined by the intersection of the X and Y axis analog voltages. The manner in which these analog voltages are developed is described in the following text.

The three LSB's of the character held in the CR register are coupled to the monoscope deflection amplifier over input lines DAX0, DAX1, DAX2. These bits are applied to a current summing network formed by Q19, Q18, Q17, and resistors R1, R2, and R3. The binary value of the three LSB's allows current to flow through various sections of the resistive network.

Depending on the character code held in the CR register, current will flow from the reference regulator through one, two, or all three of the resistors. For example: if the LSB of data in the CR register is a logic one, a logic zero (low) will be applied to the DAX0 line. Remember that the DAX0 line is connected to the zero side output of the CR register flip-flop. This low level is applied to the base of transistor Q19, cutting it off. Since Q19 is cut off current will flow through R1, thereby applying this current to the current summing line. If the input to the base of Q19 were high, Q19 would conduct, thereby acting as a short and allowing no current to flow through R1. The analog voltage applied to the base input of Q1 is therefore proportionate to the binary value of the character's three LSB's.

The three MSB's of the character held in the CR register are converted in a similar manner. These bits are applied to the monoscope deflection amplifier over input lines DAY0, DAY1, and DAY2. The Y axis summing network is formed by transistors Q22, Q21, and Q20, and resistors R42, R43, and R44. The analog voltage is applied to the base of Q9.

4-12.2 X and Y Deflection Amplifiers

The analog voltage which was generated by the digital code is amplified and applied to the deflection plates of the monoscope.

The X axis analog voltage is first applied to a differential amplifier, Q1 and Q2. The signal is applied to the base of Q1 and then is coupled from the emitter of Q1 to the emitter of Q2. The signal is then coupled through Q2 where it is again amplified by transistors Q3 and Q4. Although the analog voltage has been amplified it is still too low a level to deflect the electron beam. It is for this reason that the analog voltage is applied from Q4 to driver transistor Q6. Applied to Q6 is a +100 volt source. Therefore, sufficient voltage is provided to drive the deflection plate connected to pin J.

The second X axis deflection plate that is connected to pin K has a voltage which is inversely proportional to the voltage on the other deflection plate. This means that if the voltage on one plate is increasing the voltage on the other plate is decreasing. To accomplish this action the signal that is applied to the plate at point J is also applied to a voltage divider network composed of resistors R23 and R27. If the voltage at point J increases, the voltage drop across these two resistors will also increase. The base of Q6 is connected between R23 and R27; therefore, the voltage on the base of Q6 will increase. This increase in voltage is coupled through Q6 and Q7 where it is applied to the base of driver transistor Q7. If the voltage on the base of Q7 increases the voltage at the collector will decrease. The Y deflection amplifier will function in the same manner as did the X deflection amplifier.

The gain of the deflection amplifiers is determined by the amount of negative feedback that is applied to the inputs of the amplifiers. The gain of the X deflection amplifier is determined by the setting of R32 and the Y deflection gain is set by R50.

4-12.3 X and Y Skew Correction

The purpose of the skew correction voltage is to compensate for angular deficiencies in the X and Y deflection. A portion of the X deflection voltage is applied to the Y deflection amplifier and a portion of the Y deflection voltage is applied to the X deflection amplifier. The skew potentiometers R22 and

R69 can either add current to the summing line or subtract current from the summing line.

4-12.4 Minor Vertical Sweep Generation

The minor vertical sweep is developed in the timing circuits of A12 by a countdown circuit which divides the master clock by a factor of two. The 582 kHz squarewave signal, which is phase-shifted 180 degrees on alternate CRT scans, is applied to the base of transistor Q24. The 582 kHz squarewave is then coupled through Q24 and Q25 where it is applied to power amplifier Q3. Transistor Q3 is connected to the diddle coil (L1). The diddle coil (which produces the CRT scan horizontal line width) is a resonant circuit that changes the minor vertical squarewave signal to a sine wave. This sine wave, which occurs at a rate of 12 times per character, is applied through resistors R108 and R45 to the input to the Y axis deflection amplifier.

The minor vertical sweep is combined with the Y axis analog voltage and the X-axis skew voltage. These voltages will increase and decrease in value each time the minor vertical sine wave approaches its maximum positive or negative value. The constantly fluctuating Y axis voltages cause the monoscope beam to sweep up and down across the character symbol. This "painting" effect is phase-shifted by 180 degrees on alternate CRT scan cycles so that effectively the character symbol is scanned 24 times (12 times per frame).

4-12.5 Blank Pulse

The blank pulse circuit adds current to the X axis current summing line. Voltage is developed by the blank pulse circuit, which appears as a sawtooth waveshape. The sawtooth waveshape develops a ramp voltage that will drive the electron beam across the character to be "painted." The blank pulse circuit also inhibits any sawtooth waveform from being developed during horizontal and vertical drive.

The blank pulse circuit is composed of transistor Q23, diode CR3, and capacitor C8. The blank pulse that is applied to the base of Q23 is developed in gate A3-8 on board A12. The blank pulse is composed of three distinct pulses: $\overline{\text{CTS+1}}$, $\overline{\text{horizontal drive}}$, and $\overline{\text{vertical drive}}$.

When a $\overline{\text{CTS+1}}$ pulse is present on the blank pulse line, Q23 will conduct. When Q23 is conducting, C8 will start to discharge. Capacitor C8 will continue to discharge until the $\overline{\text{CTS+1}}$ pulse is removed from the line. When $\overline{\text{CTS+1}}$ is removed, C8 will start to charge. C8 can charge to a maximum of 22 volts as set by clamping diode CR3. Capacitor C8 will charge for 20.4 µs but will never reach full charge because of its RC time constant. The charging of C8 produces a sawtooth wave which when added to the X axis summing line drives the beam horizontally across the character. When either the $\overline{\text{horizontal drive}}$ or $\overline{\text{vertical drive}}$ pulses are applied to the base of Q23, Q23 will conduct, disabling C8 from charging. When these two pulses are removed, C8 will again start to charge. It is in this manner that a complete character is scanned from left to right.

4-13 Monoscope VI

The monoscope is a vacuum tube device that generates a video output for displaying alphanumeric and special symbols on the CRT screen.

An electron beam originating at a cathode element at one end of the tube is accelerated toward a target anode at the other end of the tube. Beam acceleration results from the difference in potential between the cathode and target anode voltages. The cathode is at a -1.2 kilovolt level developed by the high voltage power supply and the target is at 0 volts. The target anode is an aluminum oxide disc that has alphanumeric and other special symbol characters deposited in carbon. A conductive band, called a collector, is located near the target anode and around the inside perimeter of the monoscope tube. The collector is slightly more positive in potential (+3 volts) than the target anode and serves as an attractive force for pulling electrons away from the target element after secondary emission has occurred.

Electron beams accelerated toward the target anode are focused and deflected on the X and Y axes by voltages applied to X and Y electrostatic deflection plates. These deflection voltages are developed by the monoscope X and Y deflection amplifier circuits, respectively. The X deflection voltage includes a character ramp voltage and a dc analog voltage that results from the conversion of a three bit digital word. The amplitude of the dc analog voltage component is such that it deflects the beam on the horizontal axis so that the beam is positioned over one of the vertical columns of the target anode. The character ramp waveform component causes the electron beam to sweep from left to right across the width of the selected column and then retrace to the left end of the column.

The Y deflection voltage includes a 582 kHz minor vertical sweep sine wave, and a dc analog voltage that results from the conversion of a three bit digital word. The amplitude of this digital word is such that the beam is positioned on the Y axis over one of the horizontal rows on the target anode. The 582 kHz sine wave component causes the beam to move up and down the Y axis at the minor vertical rate.

With the X and Y deflection voltages simultaneously positioning the beam, the beam scans over the entire selected target character. When the beam strikes the deposited carbon portion of the character, the ratio of primary beam current to secondary emission is approximately 1:1. When, however, the beam strikes the aluminium oxide of the target anode, there is a high ratio of secondary emission to primary electrons. This ratio causes current to flow through a load resistance that is connected between the target anode and the collector. As the beam moves from carbon to aluminum oxide areas of the target, the current flowing through the load resistance varies at a rate that is determined by the character in the selected location on the target. Current flowing through the load resistance is connected to the input of a video preamplifier circuit.

4-14 Preamplifier A7

The video preamplifier, shown in figure 7-10, Raytheon Drawing 344092, amplifies the monoscope target video before coupling the video to video amplifier A8.

When the monoscope scan is directed to a character symbol on the target element, secondary emission develops a low level current of 1 to 3 microamperes. This current flows through a video compensation network formed by L1 and R4. The video is then amplified by Q1 and coupled through emitter follower Q2. The video signal is again amplified by transistor Q3. The output of Q3 is coupled through two emitter followers, Q4 and Q5, where it is applied to video amplifier A8. The output of A3 is also used as negative feedback and is applied to the emitter of Q1. The negative feedback provides dc stability.

4-15 Video Amplifier A8

The video amplifier, shown in figure 7-12, Raytheon Drawing 345406, consists of circuits that perform the following functions:

a. Amplify monoscope or cursor video levels to a level sufficient for driving the CRT cathode element. To accomplish this function transistor Q1, Q2, Q3, and Q4 are used.

b. Disable the video to the CRT when a blanking signal is present.

c. Disable video to the CRT when either the vertical or horizontal deflection amplifier fails (paragraph 4-15.3 CRT Protect).

d. Adjust the screen brightness of the CRT.

e. Develop the necessary video for displaying a cursor.

4-15.1 Video Amplification

Input video signals are coupled from the monoscope video preamplifier A7 and are applied to the base of Q1 where the video is amplified and coupled through Q2. The signal is then amplified again by Q3 and coupled in the emitter of Q4 and out the collector where it is applied to the cathode of the CRT.

4-15.2 Blanking

The CRT video is inhibited each time a blanking pulse is developed in gate A3-8 of display logic board A12. These blanking pulses occur during: CTS-1 of each character (intercharacter blanking); at the end of each line during horizontal retrace; at the end of each frame during vertical retrace.

The blanking pulse is applied through diode CR4 and added to the video line at the base of Q1. Since the blanking pulse is a positive signal, and since the video is a negative signal, they will cancel when they both occur in coincidence. This cancellation occurs during all retrace times and during intercharacter time (CTS+1).

4-15.3 CRT Protect

The CRT protect circuit prevents burning an intense vertical or horizontal line on the CRT phosphor when either CRT deflection amplifier fails. The CRT grid is normally held at a positive potential, the value of which depends upon the setting of the brightness control. When either deflection amplifier fails, a positive level is developed at the CRT Protect input. This level turns Q6 on and essentially grounds the CRT grid through the heavily conducting transistor switch Q6.

The brightness of the beam is controlled by the voltage applied to the control grid. This voltage is controlled by potentiometer R8.

4-15.4 Cursor Generation

The 582 kHz squarewave obtained from the A3 board, and the write cursor and write vertical pulses obtained from the A12 board are applied to the Q7, Q8 circuit (figure 4-30), which produces a symbol that indicates the location of the cursor. The write cursor pulse activates the Q7, Q8 circuits. The 583 kHz squarewave is differentiated, and the negative going pulses are amplified and applied to the video path in the amplifier, which generates the horizontal portion of the cursor symbol (⌋). The vertical portion is generated with the write vertical pulse which is also amplified and applied to the video patch (figure 4-11, F.).

4-16 Vertical and Horizontal Deflection Amplifier A2

The horizontal deflection amplifier receives a horizontal drive trigger from the A12 board, which starts a sawtooth generator. The resulting sawtooth is amplified and applied to horizontal deflection coil L1 as a linearly increasing current. Thus the electron beam moves horizontally across the face of the CRT screen (see figure 7-2, Raytheon Drawing 345408).

The horizontal drive pulse which goes high every 1152 μs and remains high for 144 μs is applied to the base of Q10. For the 144 μs that the horizontal drive signal is positive, Q10 conducts and appears as a short, allowing capacitor C9 to discharge. When the horizontal drive signal goes low, Q10

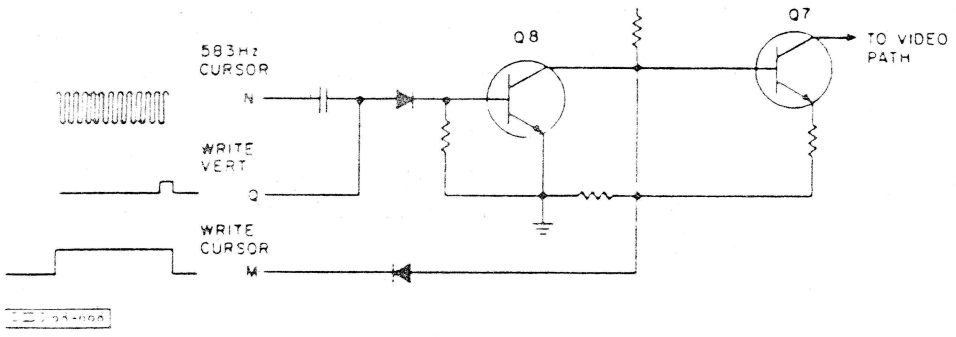


Figure 4-30. Q7, Q8 Circuit

is cut off and capacitor C9 starts to charge until the next horizontal drive pulse. C9 charges to approximately 5 volts. The charge and discharge of C9 develops a sawtooth waveform that is applied to the base of Q11. The signal is coupled out the emitter of Q11 and is applied to the base of Q12 along with a positioning voltage and a negative feedback signal. The positioning voltage which is set by R35 positions the display along the X axis. The feedback is used for stability. The sawtooth signal is amplified by Q12 and is coupled to the base of Q13 and Q14. It is important to remember that the sawtooth goes both above and below the ground level. The ground level is at the center of the sawtooth. Q13 couples that portion of the sawtooth that goes above the ground level, and Q14 couples the portion below ground. It is in this manner that both the positive and negative portions of the sawtooth are coupled to the horizontal deflection coil. The positive portion is coupled through Q13 and applied to driver transistor Q1 and through the deflection coil. During the negative portion the signal is coupled through Q14 to driver transistor Q2 and through the deflection coil. R50 is used to sample the deflection coil voltage. This sample is used as negative feedback and is also applied to the vertical deflection amplifier as a skew correction voltage.

The vertical deflection amplifier receives a vertical drive trigger from the A12 board, which starts a sawtooth generator. The resulting sawtooth is combined with a sawtooth from the horizontal deflection amplifier and applied to vertical deflection coil L1. Thus the sawtooth that drives the sweeps downward has a horizontal step for each horizontal line during the time that the horizontal sweeps occur (figure 4-11, C). The horizontal sawtooth applied to the vertical amplifier is used to correct any slant of the horizontal line caused by the downward push of the vertical deflection (figure 4-11, B). In this way, the stepped sawtooth maintains a constant vertical deflection until the end of the horizontal sweep, resulting in perfectly horizontal sweeps.

The vertical drive signal, which is positive for one horizontal line and negative for 12 line times, is applied to the base of Q1. Q1 conducts during the line time that V drive is positive. When Q1 conducts it appears as a

short and capacitor C1 discharges. When the V drive signal goes low, C1 starts to charge and will continue to charge for 12 line times. At the end of 12 line times, Q1 conducts and C1 discharges. The charge and discharge of C1 produces a sawtooth waveform that is coupled through Q2 and applied to the base of Q3 with the centering voltage, negative feedback, and the skew correction voltage. The centering voltage, which is set by R4, allows the display to be positioned along the Y axis. The skew voltage, when combined with the vertical sawtooth produces a stepped sawtooth voltage. This stepped voltage adjusts the vertical deflection sawtooth so that the CRT scan is not moved vertically until the completion of each horizontal line. This stepped sawtooth is then amplified by Q3 and applied to the base of both Q4 and Q7. Since the vertical step sawtooth goes both above and below ground, two separate amplifiers apply the signal to the vertical deflection coil. Q4 couples the signal to amplifiers Q5 and Q6 during the positive portion of the signal; and Q7, with Q8 and Q9 couples and amplifies the signal during the negative portion. Resistor R27 provides the amplifier with negative feedback.

The output of both the horizontal and vertical deflection amplifiers is applied to diodes CR11 and CR6, respectively. These two diodes form the OR gate input to the CRT protection curcuit.

4-17 Cathode Ray Tube V2

The cathode ray tube (CRT), is employed to display up to 504 high resolution characters for viewing by display terminal operators. The CRT anode is held at a potential of +12 kilovolts by a voltage developed by the high voltage power supply. A second voltage of 500 volts is applied to pin 10 as an acceleration potential. Electrons are attracted from the cathode element at a rate controlled by the setting of the brightness control

When video signals are coupled from the video amplifier, conduction through the CRT increases and a video character appears on the CRT screen. The position at which this character appears is determined by the vertical and horizontal deflection voltages applied to deflection coil L1. In addition

to the vertical and horizontal windings of the deflection coils, a minor vertical (diddle) coil is contained in L1. This coil is activated by the minor vertical signal coupled from the monoscope deflection amplifier and increases the height of each horizontal line, and therefore the character height.

CHAPTER 5

MAINTENANCE

Section I

TROUBLESHOOTING TECHNIQUES

This section contains procedures for troubleshooting to the extent of replacing circuit boards and/or replacing components mounted on or under the main chassis assembly, and procedures for removing and replacing parts.

Use the following test equipment (or equivalent) when taking measurements:

- Simpson Model 260 Multimeter (20,000 ohms/volt)
- Tektronix 545A Oscilloscope
- Tektronix type 53/54C dual trace preamplifier
- Tektronix type P6022 (10X attenuator) probe

If an oscilloscope with a narrower bandwidth capability is used, a reduction in the fidelity of the waveshape reproduction will occur. This factor should be considered when determining whether or not a board is performing properly.

5-1 Troubleshooting

The following paragraphs cover the troubleshooting methods for the high and low voltage power supplies, the analog circuits by individual circuit board, and the digital circuits.

A thorough understanding of the theory in Chapter 4 will provide the repairman with sufficient system concept to enable him to determine logically which boards or components could cause a particular fault.

5-1.1 Routine Visual Checks

Depending on the nature of the trouble, the following items should be checked:

a. Interlock switch S1 (figure 2-5)

b. Fuse F1 (figure 2-6)

c. All leads to printed circuit boards to make certain that they are properly fastended to their respective terminals.

5-1.2 Voltage Checks

Use the symptom and probable cause chart (table 5-1) to check the high and low voltage power supplies.

WARNING

Extreme caution should be exercised when making measurements on the high voltage power supply (12 kv).

a. Check the output voltages at the terminals of low voltage power supply A4 and high voltage power supply A5. The proper voltages and their respective terminals are given in figure 7-1, Raytheon Dwg 345410. Since regulation is more important than the exact value of voltage, slight variations from the prescribed voltage value should be ignored. If either power supply is faulty, it should be replaced.

Table 5-1. Power Supply Failure Chart

Sympton	Probable Cause
1. Characters moving within their character boxes	-1.2 kv unstable or excessive ripple
2. No characters displayed	-1.2 kv absent
3. Intensity of display varying and/or flashing of presentation	+22 volts unstable or excessive ripple
4. No presentation on the CRT	+22, -22, +5, +140, or -1.2 kv absent
5. CRT sweeps jumping	+100, +22 or -22 volts unstable
6. CRT sweeps unstable on right side only	+100 volts excessive ripple
7. No presentation on the CRT and the 10-ohm resistors on the horizontal and vertical deflection amplifiers A2 overheating	-22 volts unstable
8. Intensity of CRT varying and/or characters unstable in their rasters	-1.2 kv unstable
9. -1.2 kv unstable	+22 or -22 volts unstable

b. Connect an ac-coupled oscilloscope probe to each of the dc voltages in turn. With the oscilloscope gain control set for 0.5 volt/cm, observe that the trace on the oscilloscope does not move (jump). Allow the probe to remain on each voltage for two minutes to be sure that it is stable.

5-1.3 Vertical Deflection Amplifier A2 (figure 5-1 and table 5-2)

a. Check the dc voltages on the board (table 5-2).

b. Check the vertical drive (pin c). If it is not present, the trouble is not in the vertical deflection amplifier. Check the vertical drive output from display timing board A12, pin 40 (figure 7-1).

c. Check the output sweep waveform at terminal D. If improper, check deflection yoke L1 (figure 2-4) resistance and compare it with that of the spare yoke. If the deflection yoke is normal, replace amplifier A2.

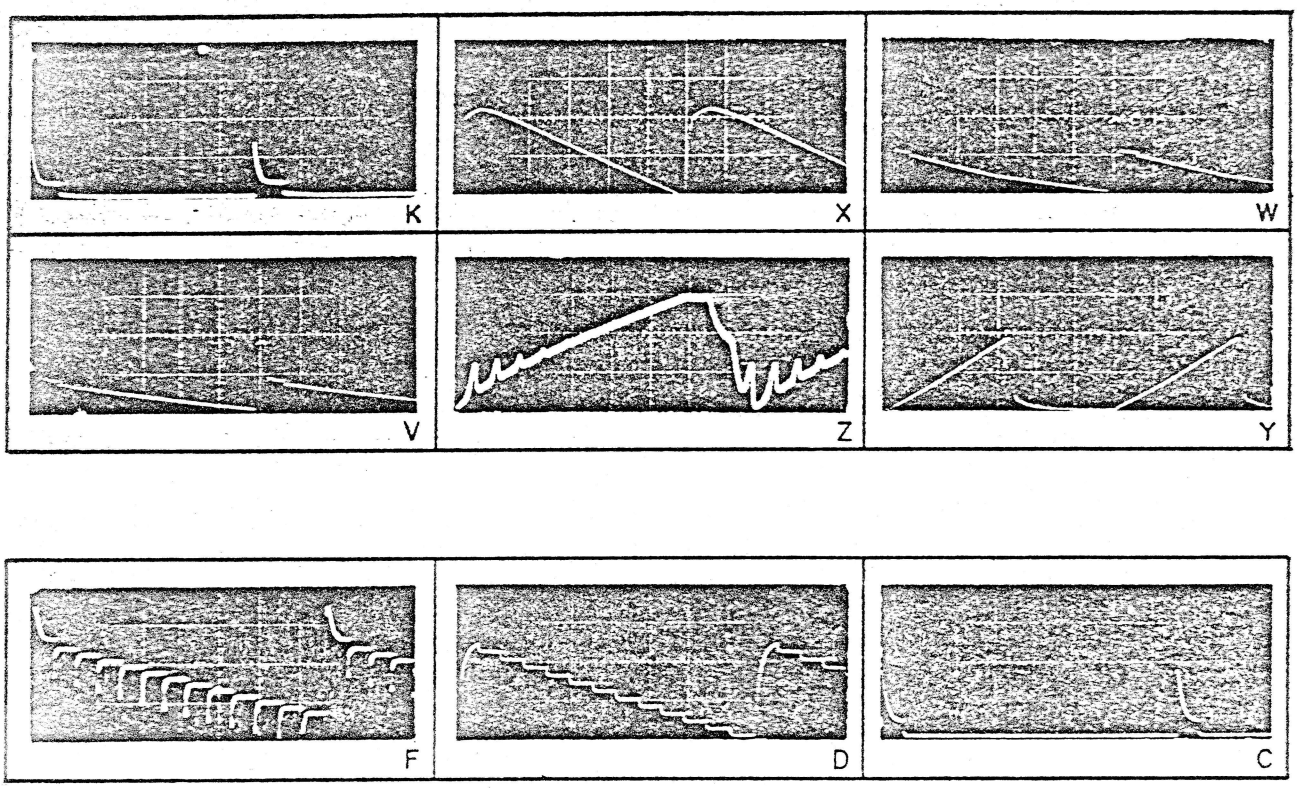


Figure 5-1. Horizontal and Vertical Deflection Amplifier A2 Waveforms

Table 5-2. Test Data, Vertical Deflection Amplifier (Part of A2)

Terminal	Sweep Speed (ms/cm)	Vertical Sensitivity (v/cm)	VDC
A			Ground
C	2.0	2.0	
D	2.0	2.0	
F	2.0	5.0	
J			Ground
N			+22
P			100
T			-22

Note: Unless otherwise noted, oscilloscope sync should be taken from vertical deflection amplifier A2, pin c.

d. Check the CRT protect at terminal G. If the voltage is more than 1 volt and the sweep output is present in the previous step, check the horizontal deflection amplifier.

e. If the deflection amplifier is replaced, the replacement board must be aligned (paragraph 2-3.3.2).

5-1.4 Horizontal Deflection Amplifier A2 (figure 5-1 and table 5-3)

Table 5-3. Test Data, Horizontal Deflection Amplifier (Part of A2)

Terminal	Sweep Speed (ms/cm)	Vertical Sensitivity (v/cm)	VDC
K	0.2	2.0	
J			Ground
A			Ground
P			100
N			+22
X	0.2	2.0	
T			-22
W	0.2	10	
V	0.2	10	
Z	2.0	0.2	
Y	0.2	5.0	

Note: Unless otherwise noted, oscilloscope sync should be taken from vertical deflection amplifier A2, pin C.

a. Check the dc voltages on the board (table 5-3).

b. Check the horizontal drive (pin K). If it is not present, the trouble is not in the horizontal deflection amplifier. Check the horizontal drive output from display timing board A12, pin 46 (figure 7-1).

c. Check the waveform at terminal W. If there is no waveshape, replace amplifier A2. If the waveshape is present at terminal W but the waveshape at terminal V is distorted, check Q1, C1, R1, and R2 and associated wiring (figure 2-3). Check deflection yoke L1 (figure 2-4) resistance and compare with that of the spare.

d. Check the waveform at terminal Y. If there is no waveshape, replace amplifier A2. If the waveshape is present at terminal Y but the waveshape at terminal V is distorted, check Q2, CR1, and R3, and associated wiring (figure 2-3).

e. Check the CRT protect at terminal Z. If the voltage is more than 1 volt and the sweep output is present at terminal V, check the vertical deflection amplifier.

f. If deflection amplifier A2 is replaced, the replacement board must be aligned (paragraph 2-3.3.2).

5-1.5 Monoscope XY Deflection Amplifier A3 (figure 5-2 and table 5-4).

a. Check the dc voltages on the board (table 5-4).

b. Check the four analog outputs to the monoscope: the Y outputs are at terminals A and B; the X outputs, at terminals J and K. Observe the notes on table 5-4. Note whether any one of these four output waveforms is different from that shown in figure 5-1. Check the minor vertical deflection signal on terminal AB. If it is absent, check the output from display timing board A12, pin 34 (figure 7-1). If it is present at terminal AB but there is no minor vertical deflection (only horizontal lines on CRT), proceed to step e.

Check for presence of the blanking signal on terminal AF. If it is not present, check the blanking output from display timing board A12, pin 52 (figure 7-1). Make sure the leads to this circuit board are properly fastened to their respective terminals. If proper signals are present, check the monoscope filament, monoscope preamplifier A7, and video amplifier A8. If proper signals are absent, proceed to the following step.

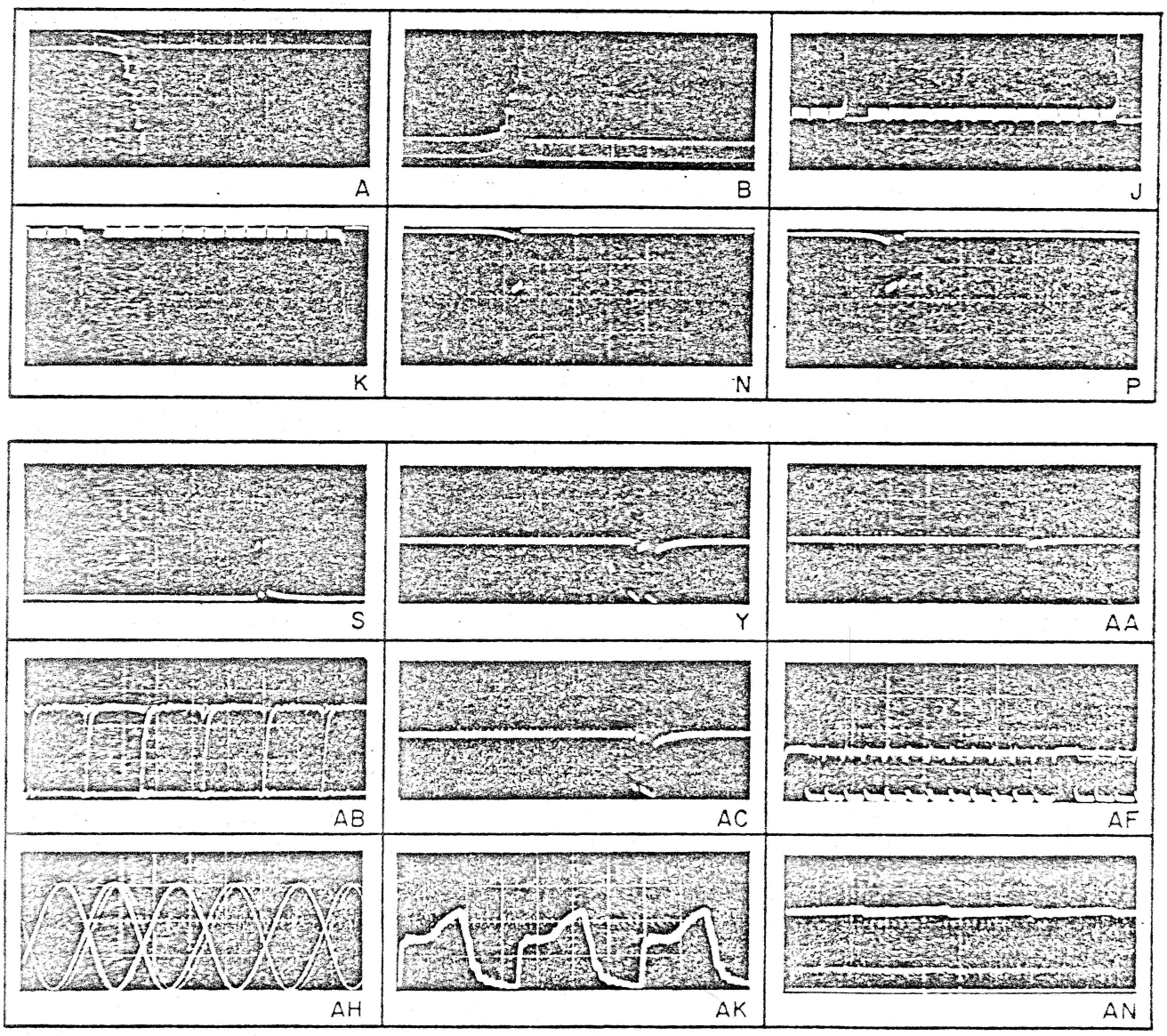


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Figure 5-2. Monoscope XY Deflection Amplifier A2 Waveforms

Table 5-4. Test Data, Monoscope XY Deflection Amplifier, A3

Terminal	Sweep Speed (ms/cm)	Vertical Sensitivity (v/cm)	VDC
A	0.2	10.0	
B	0.2	10.0	
J	2.0	10.0	
K	2.0	10.0	
N	0.2	0.5	
P	0.2	0.5	
S	0.2	0.5	
AC	0.2	0.5	
Y	0.2	0.5	
AA	0.2	0.5	
AB	0.005	0.5	
AH	0.005	10.0	
AF	2.0	1.0	
AN	0.005	2.0	
AK	0.005	1.0	
X			Ground
AD			-22
AE			+100
AM			Ground
R			+22

Note: Sync taken from vertical deflection amplifier A2 pin C. Press only the following character keys at the beginning of the frame: T G 8 1 $\overline{N}$ $\overline{R}$.

c. Check the six input digital bits as follows:

DAX0	terminal	AC
DAX1	terminal	AA
DAX2	terminal	Y
DAY0	terminal	S
DAY1	terminal	P
DAY2	terminal	N

If proper signals are present, replace monoscope XY deflection amplifier A2 and align (paragraph 2-3.3.3). If proper signals are not present, check all leads to keyboard assembly A11 and check the keyboard by substitution.

d. If replacement of circuit board A3 does not resolve the difficulty, those parts of the monoscope XY deflection circuit which are located on the indicator chassis must be checked.

(1) If the waveform at pin B is improper, check transistor Q5, resistor R5, and associated wiring (figure 2-2).

(2) If the waveform at pin A is improper, check transistor Q4, resistor R4, and associated wiring (figure 2-2).

(3) If the waveform at pin J is improper, check transistor Q6, resistor R6, and associated wiring (figure 2-2).

(4) If the waveform at pin K is improper, check transistor Q7, resistor R7, and associated wiring (figure 2-2).

e. Check the waveforms at terminals AH and AK. If waveforms are present but not proper, check transistor Q3 and wiring (figure 2-2), then check the wiring to the deflection coil and the minor vertical deflection winding on the coil. If no waveform is present at terminal AH, replace monoscope XY deflection amplifier A3. If A3 is replaced, the replacement board may require alignment (paragraph 2-3.3.3).

5-1.6 Monoscope Preamplifier A6 (table 5-5)

a. Check the dc voltages on the board (table 5-5).

b. Check the waveform at terminal A (this is the output of the pre-amplifier — the input is too small to view). If it is not present, check that all leads are properly fastened to terminals. Replace monoscope preamplifier

Table 5-5. Test Data, Monoscope Preamplifier A7

Terminal	Comment	VDC
A	See waveform A8-K (figure 5-2)	
E		Ground
B		Ground
C		-22
G		+22
F	Input from monoscope collector too small to observe	

A7. Check monoscope V1. If the signal is present (at the output of the preamplifier) troubleshoot video amplifier A8 (paragraph 2-3.3.7).

5-1.7 Video Amplifier A8 (figure 5-3 and table 5-6)

a. Check the dc voltages on the board (table 5-6).

b. Check the input waveform at terminal K. If it is not present, refer to paragraph 2-3.3.7.

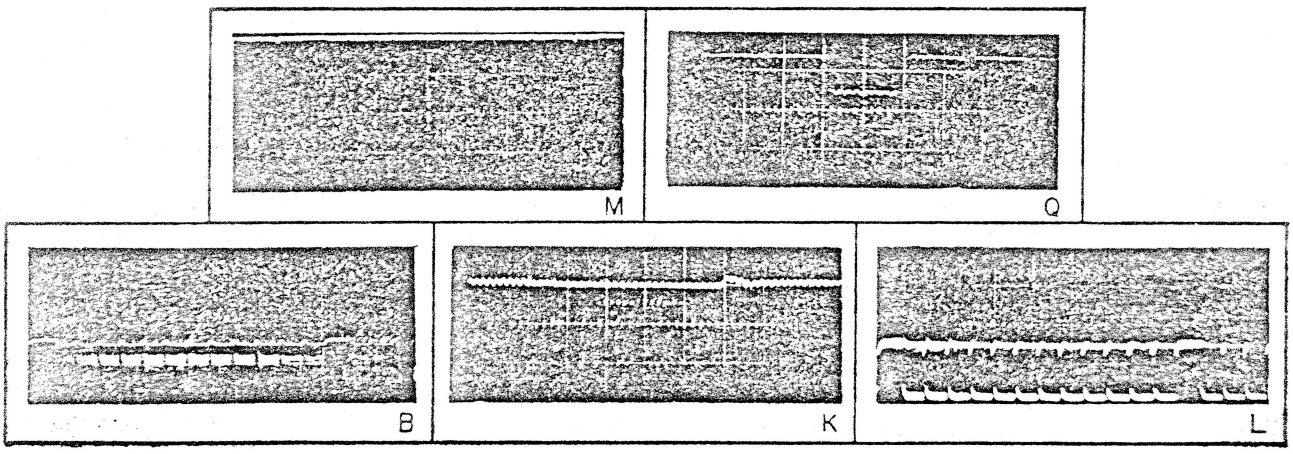


Figure 5-3. Video Amplifier A8 Waveform

Table 5-6. Test Data, Video Amplifier A8

Terminal	Sweep Speed (ms/cm)	Vertical Sensitivity (v/cm)	VDC
A			+22
B	2.0	20.0	
C			+100
D			Ground
E			*-10 to +50
F			*-10 to +50
G			-22
H	See waveform AZ-Z (figure 5-1)		
M	2.0	2.0	
N	See waveform A3-AN (figure 5-2)		
**Q	0.05 B sweep 0.0005 A sweep	0.5	
**K	0.05 B sweep 0.0005 A sweep	0.2	
I			Ground
J			Ground
L	2.0	1.0	

*Varies as Brightness Control is turned from one end to the other.
**Enter the character A in first character slot of first line. Sync the scope from the vertical drive by using the delaying sweep.

c. Check the blanking signal at terminal L. If it is not present, check the output from circuit board A12, pin 52 (figure 7-1) and wiring.

d. Check the CRT protect signal at terminal H. This waveform will be improper or the voltage more than 1 volt when either the vertical or horizontal sweep is not being generated. Troubleshoot appropriate deflection amplifier A2 (paragraph 5-1.3 or 5-1.4).

e. Check the video output waveform at terminal B. If improper, replace video amplifier A3. Adjust the video level control (paragraph 5-1.6) only if necessary.

f. Check the write vertical signal at Q. If it is not present, check the output from circuit board A12, pin 41 (figure 7-1).

g. Check the write cursor signal at M. If it is not present, check the output from circuit board A12, pin 45 (figure 7-1).

h. Check the cursor signal at N. If it is not present, check the output from circuit board A3, pin AN (figure 5-2).

5-1.8 Delay Line Electronics (figure 5-4 and table 5-7)

a. Check the dc voltage on the board (table 5-7).

b. Check the clock on terminals T, Y, V and F (figure 5-4).

c. Check the input and output signal on the board (figure 7-1).

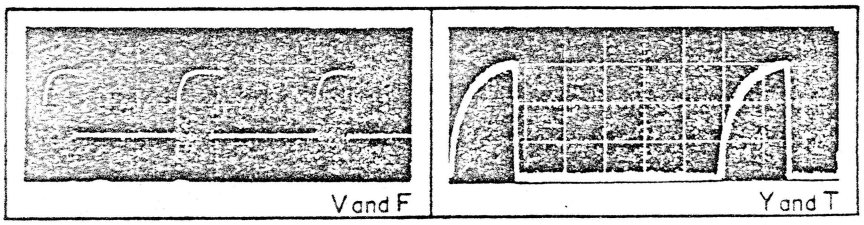


Figure 5-4. Delay Line Electronics A10 Waveforms

Table 5-7. Delay Line Electronics A10

Terminal	Sweep Speed (ms/cm)	Vertical Sensitivity (v/m)	VDC
T and Y	0.001	2.0	
V and F	0.005	1.0	
E			Ground
J			+5 volts
P			+22 volts
C			-22 volts

5-1.9 Digital Circuits

A troubleshooting chart is given in table 5-8 wherein the check procedure and corrective action is suggested for each symptom listed.

Table 5-8. Digital Circuits, Symptom Troubleshooting Chart

Symptom	Check Procedure	Corrective Action
1. Unable to write a character or characters or perform functions such as carriage return, cursor left, etc., when proper keys are pressed.	Note: Check the voltages at the terminals of the digital circuits (use figure 7-1 for identification of terminals that handle the dc voltages on the circuit boards). a. Press and hold the keys to paint the characters listed and check that the signal level changes occur at the terminals on board A12 as listed:	If functions or characters do not check out in a, b, or c, replace keyboard assembly A11. If present, replace A12.
	b. Check that strobe level at A12-13 changes when any character key is pressed. c. Check that signal level at corresponding terminals of A12 changes when frame reset (⌂), step left (←), step right (→), screen erase (BORRA), step up (↑), step down (↓), cycle right (→), cycle left (←), or ENVIA keys are pressed.	
2. Characters are entered and then disappear.	a. Adjust the delay line. b. Check the waveform at A10, pins T, Y, V, and F (see figure 1-6).	If trouble is not corrected, perform check b. If waveforms are incorrect, replace A12. If correct, replace A10 and/or A15.

Key	FX0 on 4	FX1 on 3	FX2 on 5	FY0 on 2	FY1 on 7	FY2 on 6
V	0	1	1	0	1	1
M	1	0	1	1	0	1
D	0	0	1	0	0	1
9	1	0	0	0	1	1

Table 5-8. Digital Circuits, Symptom Troubleshooting Chart (cont)

Symptom	Check Procedure	Corrective Action
3. Screen blank	a. Check horizontal and vertical drive pulses at A12-46 and A12-40. These may be checked at A2-K or A2-C.	If absent, perform check b.
	b. Check the sync line (pin 61) and the clock line (pin C4) on the A12 board.	If the signal is present, replace the A12 board. If absent, check the CU output.
	c. Check minor sweep expansion at A12-34. This may be checked at A3-AB.	If absent, replace A12.
	d. Check CRT Protect circuits (para 5-1.7d).	Follow the procedure given in para 5-1.7d.
4. No blanking between character slots.	a. Check blanking at video amplifier A8 (para 5-1.7c).	If the blanking gates are present, replace video amplifier A8. If not present, replace A12.
5. Characters change on face of display after being keyed in.		Adjust the control on the delay line for stability. If necessary, replace the delay line read-write amplifier A10, repeating step 2.
6. When a character key is pressed, a different character appears on the display.	a. Check monoscope XY deflection amplifier A3 by performing the alignment given in para 2-3.3.3.	If the six digital inputs in step 5-1.5c are correct but incorrect characters are painted even after alignment, replace monoscope XY deflection board A3.

Table 5-8. Digital Circuits, Symptom Troubleshooting Chart (cont)

Symptom	Check Procedure	Corrective Action
	b. Check the keyboard assembly as in step 1a in this Symptom Troubleshooting Chart.	If the keyboard assembly operates properly, replace board A12. If not, replace keyboard assembly A11.
7. Unable to transfer data from the control unit to the display.	a. Check the message transfer line (pin 58) and the data line (pin 68) for a signal level change.	If one or both do not change, check the CU output. If both signals change, replace the A12 board.
8. Unable to transfer data from the display to the control unit.	a. Check that a signal level change occurs at pin 76 of the A12 board when the ENVIA key is pressed.	If the signal does not change, repeat step 1a in this Symptom Troubleshooting Chart. If a signal change occurs, go to step b.
	b. Check that a signal level change occurs at pin 82 of the A12 board.	If the signal does not change, replace the A12 board. If a and b are correct, check the CU.
9. Unable to illuminate the ENVIA key when it is pressed.	a. Check that a signal level change occurs at pin 17 when the ENVIA key is pressed.	If the signal is absent, replace the A12 board. If present, replace A11.
10. Unable to display data on the Supervisor Display.	a. Check that a signal level change occurs at pin 80 of the A12 board.	If the level change is absent, replace the A12 board. If present, check the Supervisor Panel.

5-2 Removal and Replacement of Parts

Removal and replacement of most components in the DIDS-400 System is simple enough to obviate detailed instructions. A few procedures are given, however, to facilitate the repairman's task. Unless otherwise instructed, replacement procedures are the reverse of removal.

5-2.1 Removal of Cover

At the sides of the unit, remove the four screws that fasten the cover to the chassis. Remove the cover.

5-2.2 Removal of Keyboard Assembly A11

Remove the cover and unscrew the four screws located on the front plate holding the keyboard in place. Unplug the keyboard assembly.

5-2.3 Removal and Replacement of Monoscope Preamplifier A7

a. Disconnect the leads from all terminals on the monoscope preamplifier. Remove the nuts that fasten the circuit board to the chassis. Be sure to retain the spacers.

CAUTION

Pull the board out slowly to prevent breaking the lead connected to the tip of the monoscope tube.

b. Remove the lead.

5-2.4 Removal and Replacement of Circuit Boards

a. Disconnect leads from all terminals.

b. Remove all screws and washers that fasten the circuit board to the chassis.

c. To replace, fasten the circuit board to the chassis.

d. Refer to the illustration of the specific board being removed to determine the lead that fastens to each terminal as follows:

5-2.5 Removal and Replacement of CRT

a. Remove the high voltage connector on the side of the CRT.

b. Remove the connector from the rear of the tube.

c. Remove the face plate by removing four screws on main chassis, and withdraw the CRT.

5-2.6 Removal and Replacement of Deflection Yoke

a. Remove the wing nuts from the U-bracket attached to the CRT shield cover.

b. Remove the CRT (paragraph 5-3.5).

c. Draw a diagram showing the yoke lead destinations.

d. Remove the yoke wire connections.

e. Alignment consists simply of rotating the yoke for a level horizontal display after replacement.

5-2.7 Removal and Replacement of Monoscope Tube

a. Remove the preamplifier according to paragraph 5-3.3. Remove the four screws holding the logic package to the main frame. Remove the two screws holding the monoscope shield to the bottom at the rear of the chassis. Remove the two nuts holding O-clamp around the monoscope shield at the bottom of the chassis.

b. Pull the tube socket from the end of the monoscope.

c. Slide the monoscope shield to the rear for removal.

d. Remove the two screws that fasten the bracket (around the monoscope) to the shield. Slide the monoscope and the bracket out of the shield.

e. Remove the bracket and the collector lead.

f. When replacing the monoscope tube, make sure that the collector connection is on the tube aligned with the hole provided for collector lead in the shield.

5-2.8 Removal and Replacement of Delay Line A15

a. Remove the four screws holding the logic package to the main frame.

b. Remove the hardware that holds the logic board in place.

c. Disconnect the leads, unscrew the mounting hardware, and remove the delay line assembly.

5-2.9 Removal of Q4, 5, 6, and 7

Remove the four screws holding the logic package to the chassis foldout logic package. Q4, 5, 6, and 7 are located on the back of the side panel (figure 2-2).

5-2.10 Removal of Delay Line Electronics A10

Remove the delay line electronics according to paragraph 5-3.9.

5-2.11 Removal and Replacement of High Voltage Power Supply

a. Remove the four screws holding the face plate to the chassis. Remove the four screws holding the CRT assembly to chassis.

b. Remove the connector from the back of the CRT. Remove the high voltage lead. Withdraw the CRT assembly from the front of the unit.

c. Observe color coding and lead destinations; then remove the leads from the power supply. Remove the four screws holding the power supply to the bottom of the chassis. Lift the power supply from the unit.

5-2.12 Removal and Replacement of Low Voltage Power Supply

a. Remove the four screws holding the power supply to the bottom of the chassis.

b. Observe color coding and lead destinations; then remove leads from the power supply.

c. Lift the power supply from the unit.

Section II

LOGIC SYMBOLS AND DEFINITIONS

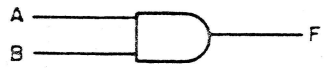
In the following list of logic symbols, explanations accompany the graphic representations.

5-3 AND Function

The symbol shown below represents the AND function.

DIDS 68-606

The AND output is high if, and only if, all the inputs are high.



DIDS 68-607

INPUT		OUTPUT
A	B	F
L	L	L
L	H	L
H	L	L
H	H	H

The symbol shown below represents one version of the AND function. The output is low if, and only if, all the inputs are high.

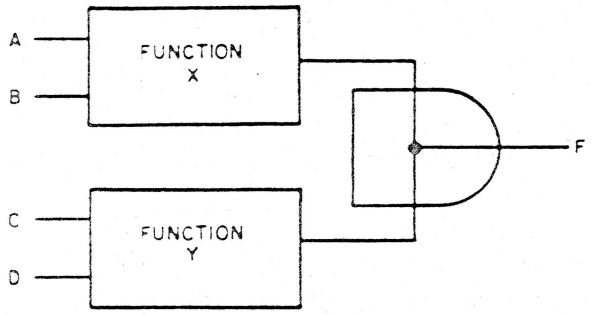
DIDS 68-608

INPUT			OUTPUT
A	B	C	F
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

*Not a part of symbol

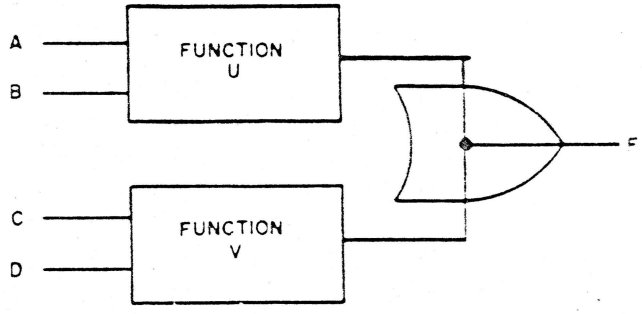
Where functions can be combined according to the AND (or OR) function simply by having the outputs connected, that capability is shown by enveloping the branched connection with a smaller sized AND or OR symbol.

Dot "AND"



DIDS [illegible]

Dot "OR"

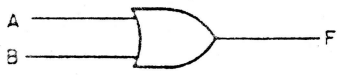


5-4 INCLUSIVE OR Function

The symbol shown below represents the INCLUSIVE OR function.

DIDS 68-609

The OR output is high (H), if, and only if, any one (or more) of the inputs is high (H).

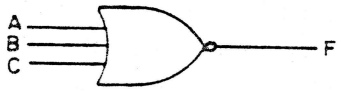


DIDS 68-610

INPUT		OUTPUT
A	B	F
L	L	L
L	H	H
H	L	H
H	H	H

*Not a part of symbol

The symbol shown below represents one version of the INCLUSIVE OR function. The output is low if any one (or more) of the inputs is high.



DIDS 68-091

INPUT			OUTPUT
A	B	C	F
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

5-5 State Indicator

State indicator (active): the presence of the small circle symbol at the input(s) or output(s) of a function indicates:

(1) Input condition: the electrical condition at the input terminal(s) which controls the active state of the respective function.

(2) Output condition: the electrical condition existing at the output terminal(s) of an activated function.

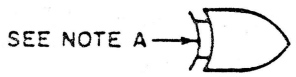
DIDS 68-012

(3) A small circle(s) at the input(s) to any element (logical or non-logical) indicates that the relatively low (L) input signal activates the function. Conversely, the absence of a small circle indicates that the relatively high (H) input signal activates the function.

(4) A small circle at the symbol output indicates that the output terminal of the activated function is relatively low (L). This small circle will never be drawn by itself on a diagram.

5-6 EXCLUSIVE OR Function

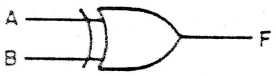
The symbol shown below represents the EXCLUSIVE OR function.



DIDS 68-092

Note A: Arc displacement determined by location of paragraph 5-8 template center input line guide hole.

The EXCLUSIVE OR output is high if, and only if, any one input is high and all other inputs are low.

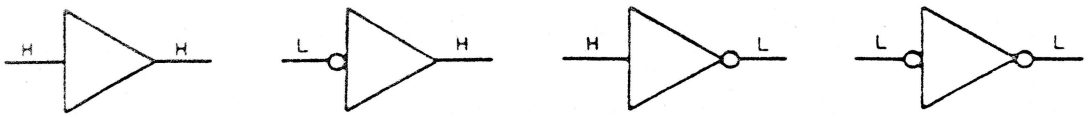


DIDS 68-093

INPUT		F = A(H) AND B(L) OR B(H) AND A(L)
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

5-7 Amplifier Symbol

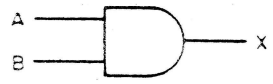
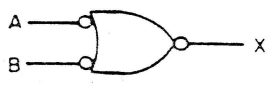
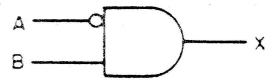
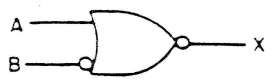
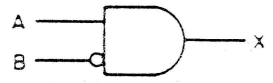
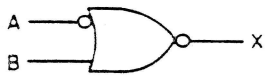
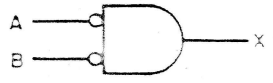
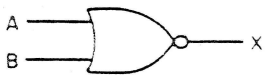
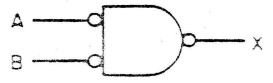
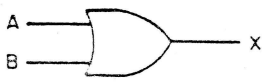
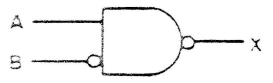
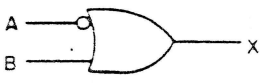
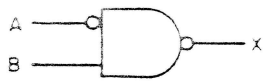
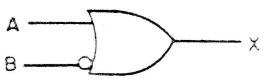
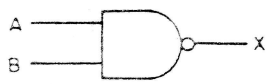
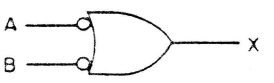
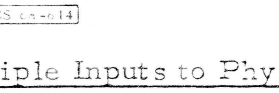
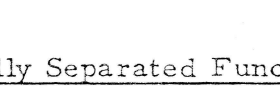
The amplifier symbol represents a linear or nonlinear current or voltage amplifier. This amplifier may have one or more stages and may or may not produce gain or inversion. Level changes and inverters, pulse amplifiers, emitter followers, cathode followers, relay pullers, lamp drivers, and shift register drivers are examples of devices for which this symbol is applicable.



DIDS 68-094

5-8 Table of Combinations

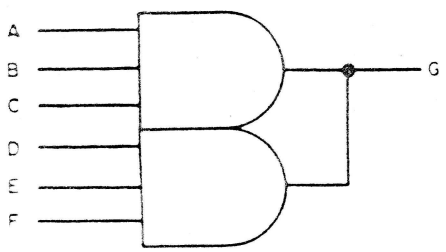
This table illustrates the application and functions of two variables and equivalents.

SYMBOLS		COMBINATIONS		
AND	OR	A	B	X
		H H L L	H L H L	H L L L
		H H L L	H L H L	L L H L
		H H L L	H L H L	L H L L
		H H L L	H L H L	L L L H
		H H L L	H L H L	H H H L
		H H L L	H L H L	H L H H
		H H L L	H L H L	H H L H
		H H L L	H L H L	H H L H
		H H L L	H L H L	L H H H

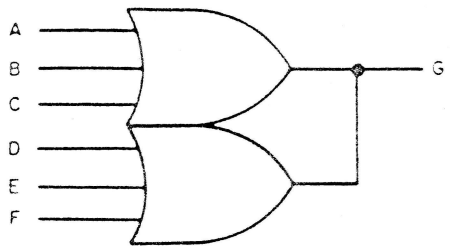
DIDS 08-014

5-9 Multiple Inputs to Physically Separated Functions with Common Outputs

AND Function



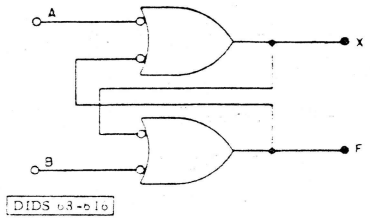
OR Function



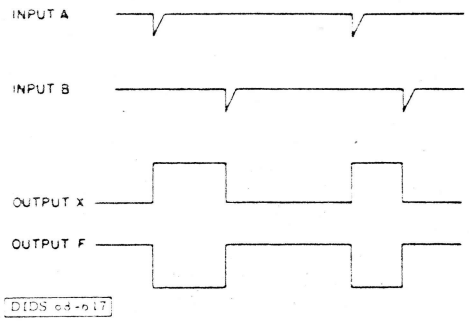
DIDS 08-015

5-10 Latch-Type Flip-Flop

The symbol shown below represents a latch-type flip-flop.

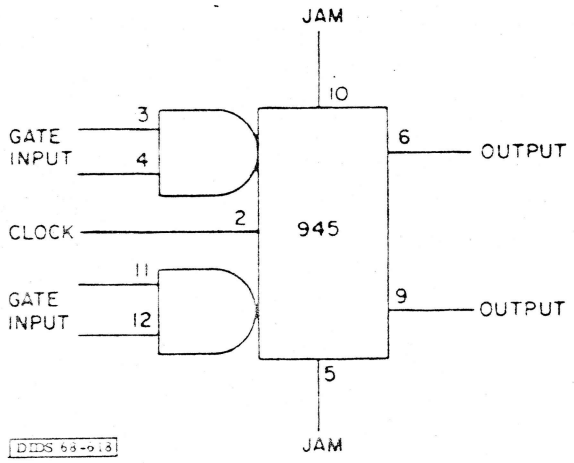


The input-output waveforms for a latch-type flip-flop are shown below.

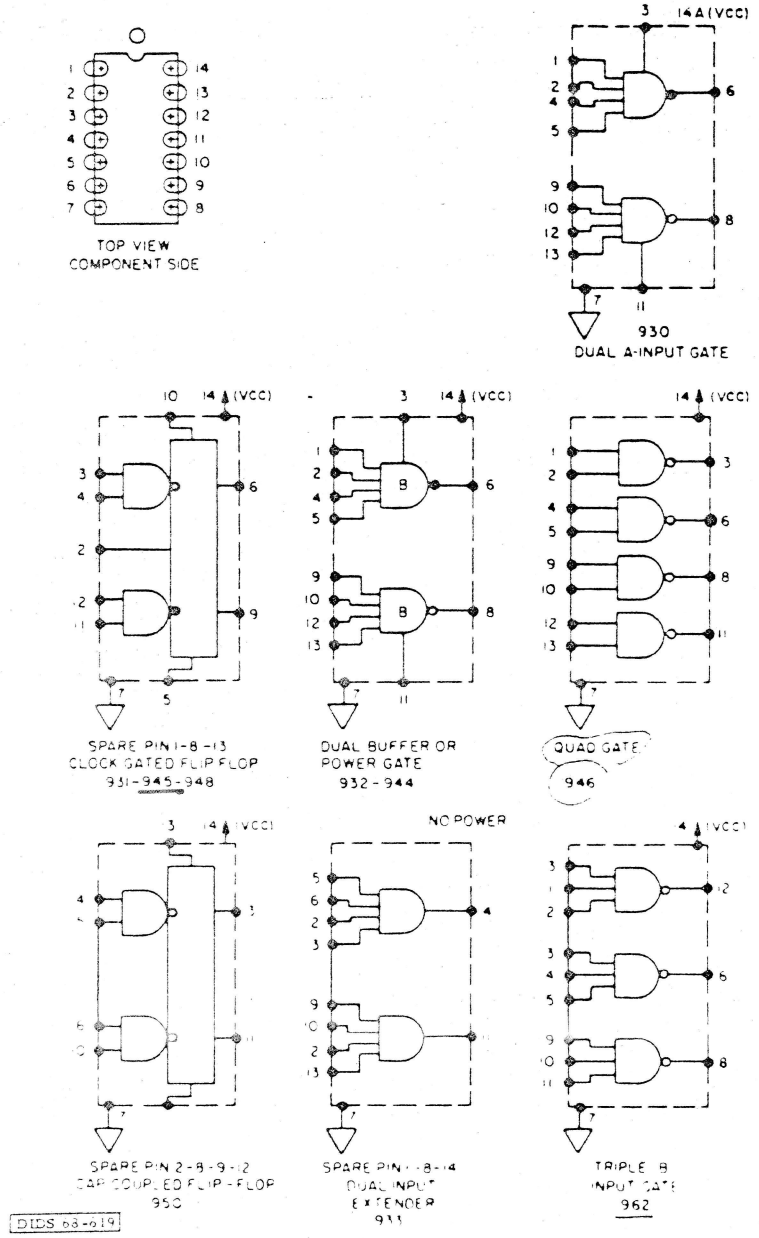


5-11 Clocked-Type Flip-Flop

The symbol shown below represents a clocked-type flip-flop. The circuit features an AND gate input and two flip-flops connected as a master-slave combination. The master flip-flop stores the input information when the clock voltage is high and transfers it to the slave when the clock voltage is low. Direct (unclocked) set and clear pulses are also provided. The unclocked pulses are used on the jam terminals of the flip-flop and will override the clocked input. A low signal on jam input pin 10 will force output pin 9 low, and a low signal on jam input pin 5 will force output pin 6 low.



5-12 Circuit Configuration and Pin Number Assignment of (DTL) Logic Elements



DIDS 68-619

DTL INTEGRATED CIRCUIT NUMBERS

ELEMENT NO.	RAYTHEON NO.
930 — 7420	329796
932 — 7440	331378
933 — 7460	329804
944 — 7440	333404
945 — 74110	329814
946 — 7400	331377
962 — 7410	331407

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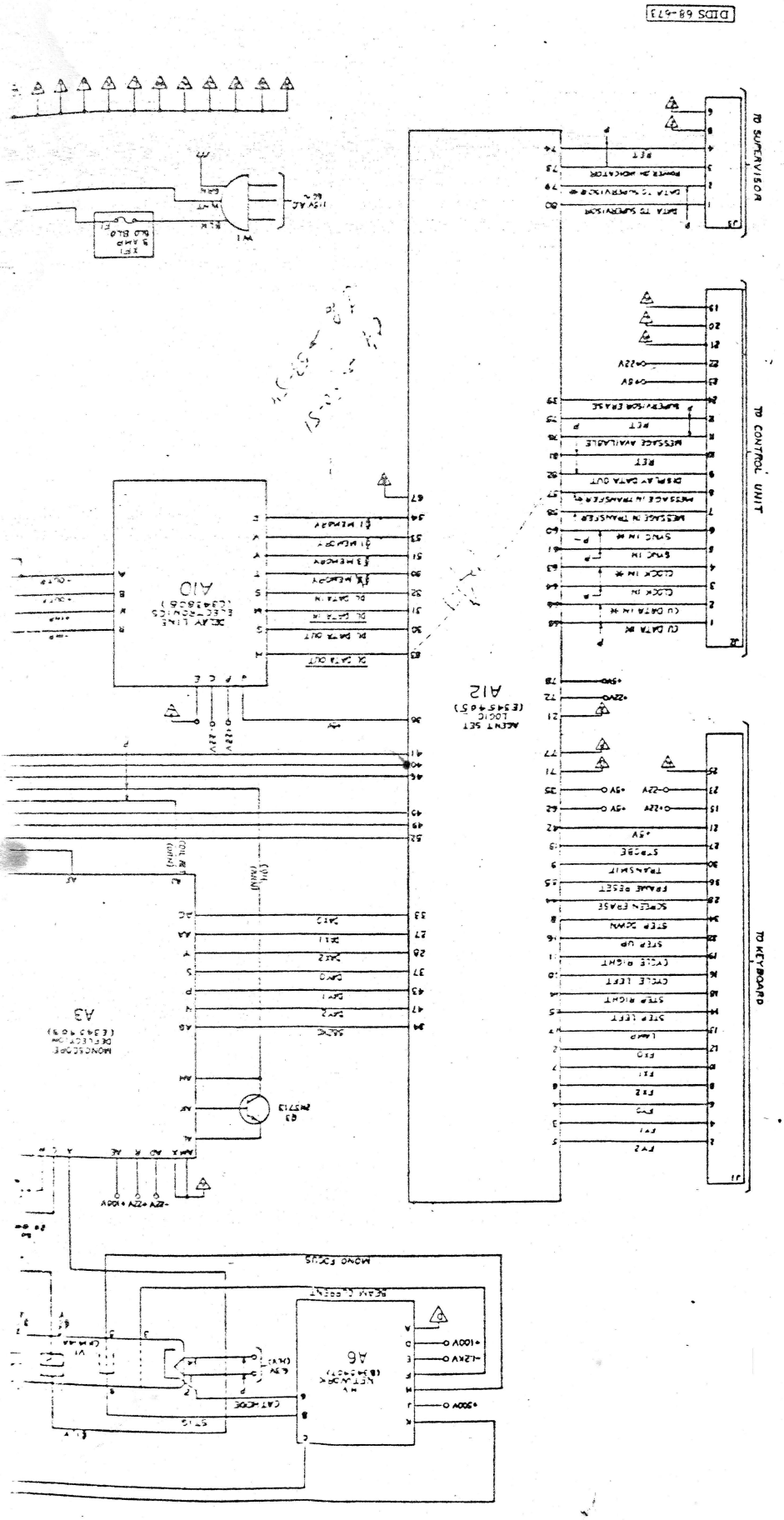
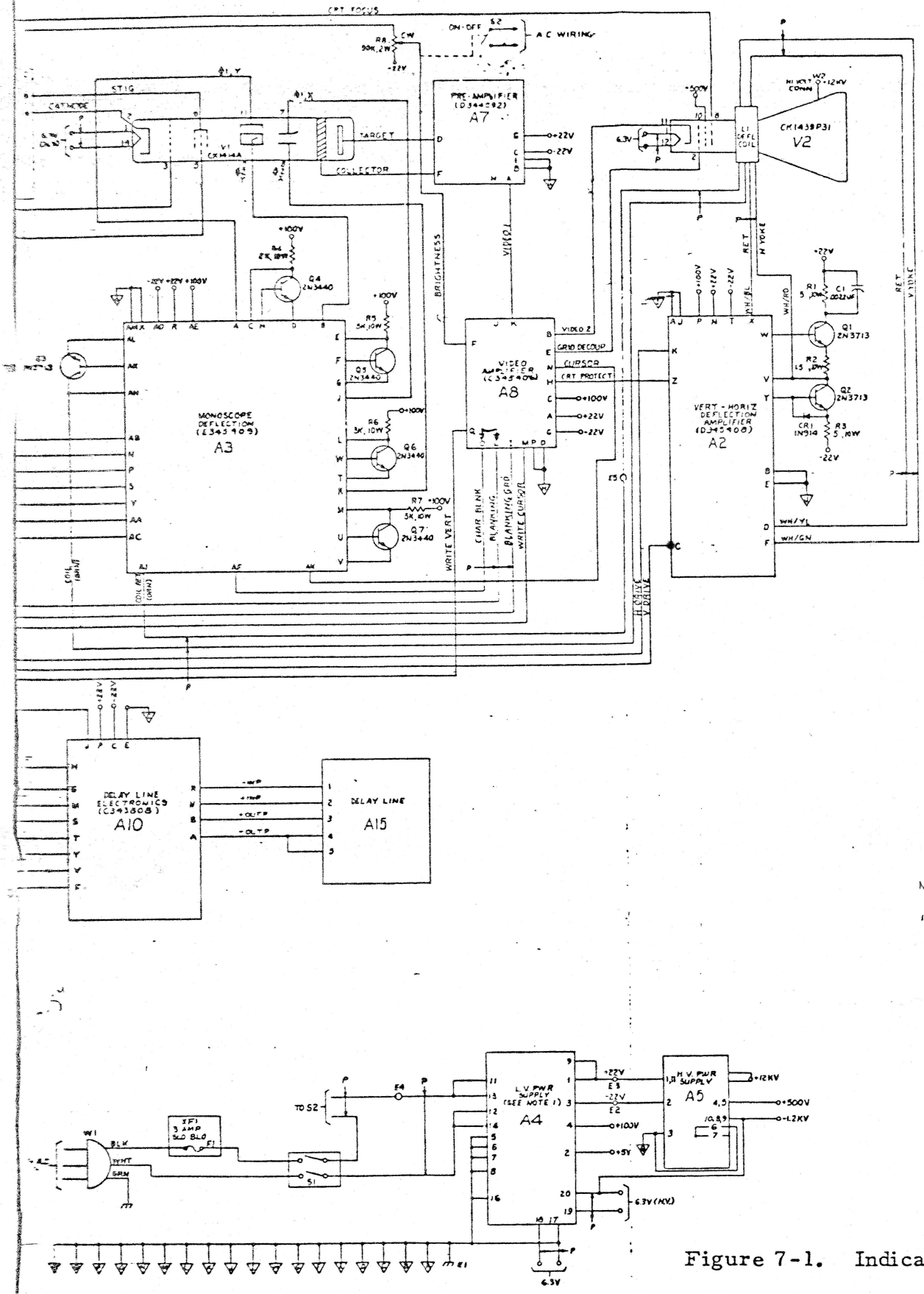

TO SUPERVISOR
TO CONTROL UNIT
TO KEYBOARD
A12
A10
A3
A6



NOTES

1. FOR 210/250V A.C. OPERATION CHANGE WIRING TO A4 AS FOLLOWS:
   a. REMOVE JUMPERS FROM 11 TO 13 & 12 TO 14
   b. ADD JUMPERS FROM 12 TO 13.
   c. CONNECT A.C. INPUT TO TERMINALS 11 & 1

Figure 7-1. Indicator Schematic 3454